Fabio Somenzi

Curriculum Vitae

January 31, 2021

Biography: Fabio Somenzi received the Dr. Eng. degree in Electronic Engineering from Politecnico di Torino, Italy, in 1980, filing a thesis on automatic test pattern generation for sequential circuits. He was with SGS-Thomson Microelectronics from 1982 to 1989 as responsible for computer-aided digital design.

From 1984 to 1987 he taught digital logic design at the Computer Science Department of the University of Milano, Italy. In 1987 he visited the Electrical Engineering and Computer Science Department of the University of California, Berkeley. Since 1989 he has been with the Department of Electrical and Computer Engineering of the University of Colorado, Boulder, where he is currently a Full Professor.

Personal Data: U.S. Citizen.

Education: Dr. Eng. Degree in Electronic Engineering (summa cum laude) Politecnico di Torino, Italy, 1980.

Professional Experience:

2001–present: Professor, Department of Electrical, Computer, and Energy Engineering University of Colorado.

1993–2001: Associate Professor, Department of Electrical and Computer Engineering University of Colorado.

1989–1993: Assistant Professor, Department of Electrical and Computer Engineering University of Colorado.

1987: Visiting Industrial Fellow, Electrical Engineering and Computer Science Department, University of California, Berkeley.

1984–1987: Adjunct Professor, Computer Science Department, Università di Milano, Italy.

1982–1989: SGS-Thomson Microelectronics, Agrate Brianza (MI), Italy. Responsible for computer aids for digital design.

1981: Served in Italian Army.

Awards:

- D'Ovidio Award as outstanding graduate of Politecnico di Torino for the academic year 1979–1980.

- Best Paper Award. Design Automation Conference, June 2000.
- Best Paper Award. Formal Methods in Computer Aided Design, November 2011.

Professional Activities:

- Associate Editor for IEEE Transactions on Computer-Aided Design (1994–1998).
- Coordinating editor for Journal of Formal Methods in System Design (2005–present).
- Reviewer for:
  - IEEE Transactions on Computer-Aided Design;
  - IEEE Transaction of Computers;
  - Journal of Formal Methods in System Design;
  - Linear Algebra and its Applications;
  - Journal of Parallel and Distributed Computing;
  - Journal of Electronic Testing Theory and Applications;
  - IEEE Design and Test;
  - IEEE Design Automation Conference;
  - IFIP VLSI Conference;
  - European Test Conference.
- Member of the Program Committee of:
  - International Conference on Computer Aided Verification (1994, 1995, 1998–2004, 2006, 2007, 2008, 2009, 2014, 2015, 2016, 2017, 2020 (Co-chair 2003)).
  - IEEE International Conference on Computer Aided Design (1989, 1992–1995, 1998, 2001–2002, 2006, 2008).
  - ACM/IEEE Design Automation Conference (1995–1997, 2007, 2008).
  - IEEE European Conference on Design Automation (1990, 1992–1994, 2001, 2003).
  - IEEE International Conference on Computer Design (1992, 1993, 1994, 1999, 2000).
  - Formal Methods in Computer-Aided Design (2006-2012).
  - IEEE European Design for Testability Workshop (1987).
  - MCNC International Workshop on Logic Synthesis (1989–2001 (Program Chair 1995, Executive Committee 1998, General Chair 1999)).
  - IFIP International Workshop on Logic and Architecture Synthesis (1990).
  - International Symposium on Low Power Electronics and Design (1996, 2000).

- International Conference on Application of Concurrency to System Design (1998).
- Computer Aided Design and Test Decision Diagrams - Concepts and Applications (1999, 2001).
- International SPIN Workshop on Model Checking of Software (2001).
- IEEE Asia-Pacific Design Automation Conference (2003).
- International Workshop on Bounded Model Checking (2004, 2005).
- IBM Verification Conference (2006).
- Workshop on Verification and Debugging (2006, co-organizer).

Ph.D. Thesis Advisor:

- H. Cho, "Reachability Analyses and Their Applications in Test Generation and Logic Optimization for Sequential Circuits," 1993.
- J.-K. Rho, "Finite State Models for the Optimization and Verification of Digital Systems," 1993.
- R. I. Bahar, "Methods for Timing Analysis and Logic Synthesis to Decrease Power Dissipation of VLSI Circuits," 1995.
- W. Lee, "Approximate Model Checking," 1998.
- K. Ravi, "Adaptive Techniques to Improve State Space Search in Formal Verification," 1999.
- M. Escobar, "Efficient Solution of Satisfiability Problems in CAD Applications," 1999.
- B. Kumthekar, "Layout Conscious Logic Optimization Techniques for Power and Delay Reduction in FPGAs," 2000.
- I.-H. Moon, "Efficient Reachability Algorithms in Symbolic Model Checking," 2000.
- R. P. Bloem, "Search Techniques and Automata for Symbolic Model Checking," 2001.
- HoonSang Jin "Efficient Algorithms for Finding All Satisfying Assignments of a Propositional Formula," 2005.
- Mohammad Awedh, "Proving properties for Bounded Model Checking" 2006.
- Bing Li, "Satisfiability-based Abstraction Refinement in Symbolic Model Checking," 2006.
- David Ward, "Exploiting High-Level Design Control and Data Structures for Hardware Verification," 2007.
- Kuntal Nanshi, "Proving Properties of Digital Systems with Abstraction-Guided Simulation," 2009.
- Hyondeuk Kim, "Efficient SMT Solving for Hardware Model Checking," 2010.

- Hyojung Han, "Increasing The Effectiveness of Deduction in Propositional SAT Solvers," 2011.
- Saqib bin Sohail, "Improving the Efficiency and Quality of Omega-Regular Synthesis," 2014.
- Zyad Hassan, "Incremental, Inductive Model Checking," 2014.
- Yan Zhang, "Statistically Sound Verification and Optimization of Black-Box Systems," 2014 (co-advised).

M.S. Student Advisor:

- Sankaranarayanan Gurumurthy
- Mitra Purandare
- Huthasana Kalyanam
- David Morgan
- Saloni Shah
- Tara Weber

Current Ph.D. Student Advisor:

- Mateo Perez, Logic Specifications for Reinforcement Learning,r (co-advised).

Research Interests. Fabio Somenzi has published two books and over 200 papers on the verification, synthesis, optimization, simulation, and testing of digital and cyberphysical systems.

References

[1] E. M. Hahn, M. Perez, S. Schewe, F. Somenzi, A. Trivedi, and D. Wojtczak. Faithful and effective reward schemes for model-free reinforcement learning of omega-regular objectives. In *ATVA: Automated Technology for Verification and Analysis*, pages 108–124, 2020. LNCS 12302.

[2] E. M. Hahn, M. Perez, S. Schewe, F. Somenzi, A. Trivedi, and D. Wojtczak. Model-free reinforcement learning for stochastic parity games. In *CONCUR: International Conference on Concurrency Theory*, pages 21:1–21:16, September 2020. LIPIcs 171.

[3] A. Lavaei, F. Somenzi, S. Soudjani, A. Trivedi, and M. Zamani. Formal controller synthesis for continuous-space MDPs via model-free reinforcement learning. In *International Conference on Cyberphysical Systems (ICCPS 2020)*, pages 98–107, April 2020.

[4] A. Lavaei, F. Somenzi, S. Soudjani, A. Trivedi, and M. Zamani. Formal controller synthesis for continuous-space MDPs via model-free reinforcement learning. *CoRR*, abs/2003.00712, 2020.

[5] E. M. Hahn, M. Perez, F. Somenzi, A. Trivedi, S. Schewe, and D. Wojtczak. Good-for-MDPs automata for probabilistic analysis and reinforcement learning. In *Tools and Algorithms for the Construction and Analysis of Systems (TACAS 20)*, pages 306–323, 2020. LNCS 12078.

[6] E. M. Hahn, M. Perez, S. Schewe, F. Somenzi, A. Trivedi, and D. Wojtczak. Reward shaping for reinforcement learning with omega-regular objectives. *CoRR*, abs/2001.05977, 2020.

[7] F. Somenzi and A. Trivedi. Reinforcement learning and formal requirements. In *Numerical Software Verification - 12th International Workshop, NSV@CAV*, pages 26–41, July 2019.

[8] E. M. Hahn, M. Perez, F. Somenzi, A. Trivedi, S. Schewe, and D. Wojtczak. Good-for-MDPs automata. *CoRR*, abs/1909.05081, 2019.

[9] E. M. Hahn, M. Perez, S. Schewe, F. Somenzi, A. Trivedi, and D. Wojtczak. Limit reachability for model-free reinforcement learning of ω-regular objectives. In *International Workshop on Symbolic-Numeric Methods for Reasoning about CPS and IoT*, 2019.

[10] E. M. Hahn, M. Perez, S. Schewe, F. Somenzi, A. Trivedi, and D. Wojtczak. Omega-regular objectives in model-free reinforcement learning. In *Tools and Algorithms for the Construction and Analysis of Systems (TACAS 19)*, pages 395–412, 2019. LNCS 11427.

[11] E. M. Hahn, M. Perez, S. Schewe, F. Somenzi, A. Trivedi, and D. Wojtczak. Omega-regular objectives in model-free reinforcement learning. *CoRR*, abs/1810.00950, 2018.

[12] F. Somenzi, B. Touri, and A. Trivedi. Almost-sure reachability in stochastic multi-mode systems. In *ACM International Conference on Hybrid Systems (HSCC18)*, pages 11–20, April 2018.

[13] S. N. Krishna, A. Kumar, F. Somenzi, B. Touri, and A. Trivedi. The reach-avoid problem for constant-rate multi-mode systems. In *Automated Technology for Verification and Analysis - 15th International Symposium, ATVA*, pages 463–479, Pune, India, October 2017.

[14] S. N. Krishna, A. Kumar, F. Somenzi, B. Touri, and A. Trivedi. The reach-avoid problem for constant-rate multi-mode systems. *CoRR*, abs/1707.04151, 2017.

[15] F. Somenzi, B. Touri, and A. Trivedi. Almost-Sure Reachability in Stochastic Multi-Mode System. *ArXiv e-prints 1610.05412*, October 2016.

[16] M. Dooley and F. Somenzi. Proving parameterized systems safe by generalizing clausal proofs of small instances. In *Computer Aided Verification*, pages 292–309, Toronto, Canada, July 2016.

[17] Y. Zhang, S. Sankaranarayanan, and F. Somenzi. Statistically sound verification and optimization for complex systems. In *Automated Technology for Verification and Analysis (ATVA)*, pages 411–427, November 2014. LNCS 8837.

[18] Y. Zhang, S. Sankaranarayanan, and F. Somenzi. Sparse statistical model inference for analog circuits under process variations. In *Asia and South Pacific Design Automation Conference*, pages 449–454, Singapore, January 2014.

[19] Z. Hassan, A. R. Bradley, and F. Somenzi. Better generalization in IC3. In *Formal Methods in Computer Aided Design*, pages 157–164, Portland, OR, November 2013.

[20] S. Sohail and F. Somenzi. Efficient handling of obligation constraints in synthesis from omega-regular specifications. In *Formal Methods in Computer Aided Design*, pages 34–41, Portland, OR, November 2013.

[21] S. Sohail and F. Somenzi. Safety first: A two-stage algorithm for the synthesis of reactive systems. *Software Tools for Technology Transfer*, 15(5-6):433–454, 2013.

[22] Y. Zhang, S. Sankaranarayanan, F. Somenzi, X. Chen, and E. Ábráham. From statistical model checking to statistical model inference: Characterizing the effect of process variations in analog circuits. In *Proceedings of the International Conference on Computer-Aided Design*, pages 662–669, San Jose, CA, November 2013.

[23] K. Nanshi and F. Somenzi. Using abstraction to guide the search for long error traces. *IEEE Transactions on Computer-Aided Design*, 32(3):453–466, March 2013.

[24] Y. Zhang, S. Sankaranarayanan, and F. Somenzi. Piecewise linear modeling of nonlinear devices for formal verification of analog circuits. In *Formal Methods in Computer Aided Design (FMCAD)*, pages 196–203, Oxford, UK, October 2012.

[25] Z. Hassan, A. R. Bradley, and F. Somenzi. Incremental inductive CTL model checking. In *Computer Aided Verification (CAV)*, pages 532–547, Berkeley, CA, July 2012. LNCS 7358.

[26] F. Somenzi and A. R. Bradley. IC3: Where monolithic and incremental meet. In *Formal Methods in Computer Aided Design (FMCAD'11)*, pages 3–8, Austin, TX, November 2011.

[27] A. R. Bradley, F. Somenzi, Z. Hassan, and Y. Zhang. An incremental approach to model checking progress properties. In *Formal Methods in Computer Aided Design (FMCAD'11)*, pages 144–153, Austin, TX, November 2011.

[28] Z. Hassan, Y. Zhang, and F. Somenzi. A study of sweeping algorithms in the context of model checking. In *First International Workshop on Design and Implementation of Formal Tools and Systems (DIFTS 2011)*, pages 30–37, Austin, TX, November 2011.

[29] H. Kim, F. Somenzi, and H. Jin. Selective SMT encoding for hardware model checking. In *9th International Workshop on Satisfiability Modulo Theories (SMT 2011)*, Snowbird, UT, July 2011.

[30] H. Han, H. Jin, and F. Somenzi. Clause simplification through dominator analysis. In *Design, Automation and Test in Europe (DATE 2011)*, pages 143–148, Grenoble, France, March 2011.

[31] H. Han, F. Somenzi, and H. Jin. Making deduction more effective in SAT solvers. *IEEE Transactions on Computer-Aided Design*, 29(8):1271–1284, August 2010.

[32] S. Sohail and F. Somenzi. A two-stage algorithm for LTL games. In *Ninth International Conference on Formal Methods in Computer-Aided Design (FMCAD 2009)*, pages 77–84, Austin, TX, November 2009.

[33] K. Nanshi and F. Somenzi. Constraints in one-to-many concretization for abstraction refinement. In *Proceedings of the Design Automation Conference*, pages 569–574, San Francisco, CA, July 2009.

[34] H. Kim, F. Somenzi, and H. Jin. Efficient term-ITE conversion for satisfiability modulo theories. In *Twelfth International Conference on Theory and Applications of Satisfiability Testing (SAT 2009)*, pages 195–208, Swansea, UK, June 2009. Springer-Verlag. LNCS 5584.

[35] H. Han and F. Somenzi. On-the-fly clause improvement. In *Twelfth International Conference on Theory and Applications of Satisfiability Testing (SAT 2009)*, pages 209–222, Swansea, UK, June 2009. Springer-Verlag. LNCS 5584.

[36] H. Kim, H. Jin, K. Ravi, P. Spacek, J. Pierce, R. P. Kurshan, and F. Somenzi. Application of formal word-level analysis to constrained random simulation. In *Twentieth Conference on Computer Aided Verification (CAV'08)*, pages 487–490, Princeton, NJ, July 2008. LNCS 5123.

[37] K. Nanshi and F. Somenzi. Improved visibility in one-to-many trace concretization. In *Design Automation and Test in Europe*, pages 819–824, Munich, Germany, March 2008.

[38] S. Sohail, F. Somenzi, and K. Ravi. A hybrid algorithm for LTL games. In *Verification, Model Checking and Abstract Interpretation*, pages 309–323, San Francisco, CA, January 2008. LNCS 4905.

[39] H. Kim, H. Jin, and F. Somenzi. Disequality management in integer difference logic via finite instantiations. *Journal on Satisfiability, Boolean Modeling and Computation*, 3:47–66, 2007.

[40] H. Han and F. Somenzi. Alembic: An efficient algorithm for CNF preprocessing. In *Proceedings of the Design Automation Conference*, pages 582–587, San Diego, CA, June 2007.

[41] D. Ward and F. Somenzi. Decomposing image computation for symbolic reachability analysis using control flow information. In *Proceedings of the International Conference on Computer-Aided Design*, pages 779–785, San Jose, CA, November 2006.

[42] H. Kim and F. Somenzi. Finite instantiations for integer difference logic. In *Formal Methods in Computer Aided Design (FMCAD'06)*, pages 31–38, San Jose, CA, November 2006.

[43] M. Awedh and F. Somenzi. Automatic invariant strengthening to prove properties in bounded model checking. In *Proceedings of the Design Automation Conference*, pages 1073–1076, San Francisco, CA, July 2006.

[44] K. Nanshi and F. Somenzi. Guiding simulation with increasingly refined abstract traces. In *Proceedings of the Design Automation Conference*, pages 737–742, San Francisco, CA, July 2006.

[45] C. Wang, G. D. Hachtel, and F. Somenzi. *Abstraction Refinement for Large Scale Model Checking*. Springer, 2006.

[46] C. Wang, B. Li, H. Jin, G. D. Hachtel, and F. Somenzi. Fine-grain abstraction and SOR guided refinement for large scale model checking. *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, 25(11):2297–2316, 2006.

[47] C. Wang, R. Bloem, K. Ravi, G. D. Hachtel, and F. Somenzi. Compositional SCC analysis for language emptiness checking. *Journal of Formal Methods in System Design*, 28(1):5–26, 2006.

[48] A. Kuehlmann and F. Somenzi. Equivalence checking. In L. Scheffer, L. Lavagno, and G. Martin, editors, *Electronic Design Automation for Integrated Circuits Handbook*. CRC Press, 2006.

[49] B. Li and F. Somenzi. Efficient abstraction refinement in interpolation-based unbounded model checking. In *International Conference on Tools and Algorithms for Construction and Analysis of Systems (TACAS'06)*, pages 227–241, Vienna, Austria, March 2006. LNCS 3920.

[50] H. Jin and F. Somenzi. Strong conflict analysis for propositional satisfiability. In *Design, Automation and Test in Europe (DATE'06)*, pages 818–823, Munich, Germany, March 2006.

[51] R. Bloem, H. N. Gabow, and F. Somenzi. An algorithm for strongly connected component analysis in $n \log n$ symbolic steps. *Formal Methods in System Design*, 28(1):37–56, January 2006.

[52] D. Ward and F. Somenzi. Automatic generation of hints for symbolic traversal. In *Correct Hardware Design and Verification Methods (CHARME'05)*, pages 207–221, Saarbrucken, Germany, October 2005. Springer-Verlag. LNCS 3725.

[53] M. Awedh and F. Somenzi. Termination criteria for bounded model checking: Extensions and comparison. *Electronic Notes in Theoretical Computer Science*, 144(1):51–66, 2006. Presented at the Third International Workshop on Bounded Model Checking (BMC'05).

[54] H. Jin and F. Somenzi. Prime clauses for fast enumeration of satisfying assignments to Boolean circuits. In *Proceedings of the Design Automation Conference*, pages 750–753, Anaheim, CA, June 2005.

[55] H. Jin, H. Han, and F. Somenzi. Efficient conflict analysis for finding all satisfying assignments of a Boolean circuit. In *International Conference on Tools and Algorithms for Construction and Analysis of Systems (TACAS'05)*, pages 287–300, April 2005. LNCS 3440.

[56] B. Li, C. Wang, and F. Somenzi. Abstraction refinement in symbolic model checking using satisfiability as the only decision procedure. *Software Tools for Technology Transfer*, 7(2):143–155, April 2005.

[57] B. Li and F. Somenzi. Efficient computation of small abstraction refinements. In *Proceedings of the International Conference on Computer-Aided Design*, pages 518–525, San Jose, CA, November 2004.

[58] M. Awedh and F. Somenzi. Increasing the robustness of bounded model checking by computing lower bounds on the reachable states. In *Formal Methods in Computer Aided Design*, pages 230–244, Austin, TX, November 2004. Springer. LNCS 3312.

[59] C. Wang, G. D. Hachtel, and F. Somenzi. Fine-grain abstraction and sequential don't cares for large scale model checking. In *Proceedings of the International Conference on Computer Design*, pages 112–118, San Jose, CA, October 2004.

[60] H. Jin, K. Ravi, and F. Somenzi. Fate and free will in error traces. *Software Tools for Technology Transfer*, 6(2):102–116, August 2004.

[61] H. Jin and F. Somenzi. An incremental algorithm to check satisfiability for bounded model checking. *Electronic Notes in Theoretical Computer Science*, 2004. Second International Workshop on Bounded Model Checking. http://www.elsevier.nl/locate/entcs/.

[62] M. Awedh and F. Somenzi. Proving more properties with bounded model checking. In R. Alur and D. Peled, editors, *Sixteenth Conference on Computer Aided Verification (CAV'04)*, pages 96–108. Springer-Verlag, Berlin, July 2004. LNCS 3114.

[63] H. Jin, M. Awedh, and F. Somenzi. CirCUs: A satisfiability solver geared towards bounded model checking. In R. Alur and D. Peled, editors, *Sixteenth Conference on Computer Aided Verification (CAV'04)*, pages 519–522. Springer-Verlag, Berlin, July 2004. LNCS 3114.

[64] C. Wang, H. Jin, G. D. Hachtel, and F. Somenzi. Refining the SAT decision ordering for bounded model checking. In *Proceedings of the Design Automation Conference*, pages 535–538, San Diego, CA, June 2004.

[65] H. Jin and F. Somenzi. CirCUs: A hybrid satisfiability solver. In *International Conference on Theory and Applications of Satisfiability Testing (SAT 2004)*, Vancouver, Canada, May 2004.

[66] K. Ravi and F. Somenzi. Minimal assignments for bounded model checking. In *International Conference on Tools and Algorithms for Construction and Analysis of Systems (TACAS'04)*, pages 31–45, Barcelona, Spain, March-April 2004. LNCS 2988.

[67] C. Wang, B. Li, H. Jin, G. D. Hachtel, and F. Somenzi. Improving Ariadne's bundle by following multiple threads in abstraction refinement. In *Proceedings of the International Conference on Computer-Aided Design*, pages 408–415, November 2003.

[68] C. Wang, G. D. Hachtel, and F. Somenzi. The compositional far side of image computation. In *Proceedings of the International Conference on Computer-Aided Design*, pages 334–340, November 2003.

[69] F. Somenzi. The charme of abstract entities. In *Correct Hardware Design and Verification Methods (CHARME'03)*, page 2, Berlin, October 2003. Springer-Verlag. LNCS 2860.

[70] S. Gurumurthy, O. Kupferman, F. Somenzi, and M. Y. Vardi. On complementing nondeterministic Büchi automata. In *Correct Hardware Design and Verification Methods (CHARME'03)*, pages 96–110, Berlin, October 2003. Springer-Verlag. LNCS 2860.

[71] B. Li, C. Wang, and F. Somenzi. A satisfiability-based approach to abstraction refinement in model checking. *Electronic Notes in Theoretical Computer Science*, 89(4), 2003. First International Workshop on Bounded Model Checking. http://www.elsevier.nl/locate/entcs/volume89.html.

[72] N. Jayakumar, M. Purandare, and F. Somenzi. Dos and don'ts of CTL state coverage estimation. In *Proceedings of the Design Automation Conference*, pages 292–295, Anaheim, CA, June 2003.

[73] F. Somenzi, K. Ravi, and R. Bloem. Analysis of symbolic SCC hull algorithms. In M. D. Aagaard and J. W. O'Leary, editors, *Formal Methods in Computer Aided Design*, pages 88–105. Springer-Verlag, November 2002. LNCS 2517.

[74] M. Purandare and F. Somenzi. Vacuum cleaning CTL formulae. In E. Brinksma and K. G. Larsen, editors, *Fourteenth Conference on Computer Aided Verification (CAV'02)*, pages 485–499. Springer-Verlag, Berlin, July 2002. LNCS 2404.

[75] S. Gurumurthy, R. Bloem, and F. Somenzi. Fair simulation minimization. In E. Brinksma and K. G. Larsen, editors, *Fourteenth Conference on Computer Aided Verification (CAV'02)*, pages 610–623. Springer-Verlag, Berlin, July 2002. LNCS 2404.

[76] H. Jin, K. Ravi, and F. Somenzi. Fate and free will in error traces. In *International Conference on Tools and Algorithms for Construction and Analysis of Systems (TACAS'02)*, pages 445–459, Grenoble, France, April 2002. LNCS 2280.

[77] H. Jin, A. Kuehlmann, and F. Somenzi. Fine-grain conjunction scheduling for symbolic reachability analysis. In *International Conference on Tools and Algorithms for Construction and Analysis of Systems (TACAS'02)*, pages 312–326, Grenoble, France, April 2002. LNCS 2280.

[78] C. Wang, R. Bloem, G. D. Hachtel, K. Ravi, and F. Somenzi. Divide and compose: SCC refinement for language emptiness. In *International Conference on Concurrency Theory (CONCUR01)*, pages 456–471, Berlin, August 2001. Springer-Verlag. LNCS 2154.

[79] F. Somenzi. Efficient manipulation of decision diagrams. *Software Tools for Technology Transfer*, 3(2):171–181, 2001.

[80] R. Drechsler, W. Günther, and F. Somenzi. Using lower bounds during dynamic BDD minimization. *IEEE Transactions on Computer-Aided Design*, 20(1):51–57, January 2001.

[81] M. A. Breuer, M. Sarrafzadeh, and F. Somenzi. Fundamental CAD algorithms. *IEEE Transactions on Computer-Aided Design*, 19(12), December 2000.

[82] R. Bloem, H. N. Gabow, and F. Somenzi. An algorithm for strongly connected component analysis in $n \log n$ symbolic steps. In W. A. Hunt, Jr. and S. D. Johnson, editors, *Formal Methods in Computer Aided Design*, pages 37–54. Springer-Verlag, November 2000. LNCS 1954.

[83] I-H. Moon, G. D. Hachtel, and F. Somenzi. Border-block triangular form and conjunction schedule in image computation. In W. A. Hunt, Jr. and S. D. Johnson, editors, *Formal Methods in Computer Aided Design*, pages 73–90. Springer-Verlag, November 2000. LNCS 1954.

[84] K. Ravi, R. Bloem, and F. Somenzi. A comparative study of symbolic algorithms for the computation of fair cycles. In W. A. Hunt, Jr. and S. D. Johnson, editors, *Formal Methods in Computer Aided Design*, pages 143–160. Springer-Verlag, November 2000. LNCS 1954.

[85] R. Bloem, I.-H. Moon, K. Ravi, and F. Somenzi. Approximations for fixpoint computations in symbolic model checking. In *In Proceedings of the World Multiconference on Systemics, Cybernetics and Informatics (SCI2000), Volume VIII, Part II*, pages 701–706, Orlando, FL, July 2000.

[86] F. Somenzi and R. Bloem. Efficient Büchi automata from LTL formulae. In E. A. Emerson and A. P. Sistla, editors, *Twelfth Conference on Computer Aided Verification (CAV'00)*, pages 248–263. Springer-Verlag, Berlin, July 2000. LNCS 1855.

[87] I.-H. Moon, J. H. Kukula, K. Ravi, and F. Somenzi. To split or to conjoin: The question in image computation. In *Proceedings of the Design Automation Conference*, pages 23–28, Los Angeles, CA, June 2000.

[88] R. Bloem, K. Ravi, and F. Somenzi. Symbolic guided search for CTL model checking. In *Proceedings of the Design Automation Conference*, pages 29–34, Los Angeles, CA, June 2000.

[89] G. Cabodi, S. Quer, and F. Somenzi. Optimizing sequential verification by retiming transformations. In *Proceedings of the Design Automation Conference*, pages 601–606, Los Angeles, CA, June 2000.

[90] C. Meinel, F. Somenzi, and T. Theobald. Linear sifting of decision diagrams and its application in synthesis. *IEEE Transactions on Computer-Aided Design*, 19(5):521–533, May 2000.

[91] B. Kumthekar, L. Benini, E. Macii, and F. Somenzi. Power optimisation of FPGA-based designs without rewiring. *IEE Proceedings on Computers and Digital Techniques*, 147(3):167–174, May 2000.

[92] B. Kumthekar and F. Somenzi. Power and delay reduction via simultaneous logic and placement optimization in FPGAs. In *Proceedings of the Conference on Design, Automation and Test in Europe*, pages 202–207, Paris, France, March 2000.

[93] I.-H. Moon, J. Kukula, T. Shiple, and F. Somenzi. Least fixpoint approximations for reachability analysis. In *Proceedings of the International Conference on Computer-Aided Design*, pages 41–44, San Jose, CA, November 1999.

[94] H. Higuchi and F. Somenzi. Lazy group sifting for efficient symbolic state traversal of FSMs. In *Proceedings of the International Conference on Computer-Aided Design*, pages 45–49, San Jose, CA, November 1999.

[95] K. Ravi and F. Somenzi. Efficient fixpoint computation for invariant checking. In *Proceedings of the International Conference on Computer Design*, pages 467–474, Austin, TX, October 1999.

[96] K. Ravi and F. Somenzi. Hints to accelerate symbolic traversal. In *Correct Hardware Design and Verification Methods (CHARME'99)*, pages 250–264, Berlin, September 1999. Springer-Verlag. LNCS 1703.

[97] F. Somenzi. Symbolic state exploration. *Electronic Notes in Theoretical Computer Science*, 23, 1999. http://www.elsevier.nl/locate/entcs/volume23.html.

[98] R. Bloem, K. Ravi, and F. Somenzi. Efficient decision procedures for model checking of linear time logic properties. In N. Halbwachs and D. Peled, editors, *Eleventh Conference on Computer Aided Verification (CAV'99)*, pages 222–235. Springer-Verlag, Berlin, 1999. LNCS 1633.

[99] I.-H. Moon, J. Kukula, T. Shiple, and F. Somenzi. Least fixpoint MBM: Improved technique for approximate reachability. Presented at IWLS99, Lake Tahoe, CA, June 1999.

[100] B. Kumthekar and F. Somenzi. Experiments on flexibilities for logic and routing optimization in FPGAs. Presented at IWLS99, Lake Tahoe, CA, June 1999.

[101] F. Somenzi. Binary decision diagrams. In M. Broy and R. Steinbrüggen, editors, *Calculational System Design*, pages 303–366. IOS Press, Amsterdam, 1999.

[102] R. K. Ranjan, V. Singhal, F. Somenzi, and R. K. Brayton. Using combinational verification for sequential circuits. In *Proceedings of the Conference on Design Automation and Test in Europe (DATE99)*, Munich, Germany, March 1999.

[103] E. Macii, M. Pedram, and F. Somenzi. High-level power modeling, estimation, and optimization. *IEEE Transactions on Computer-Aided Design*, 17(11):1061–1079, November 1998.

[104] B. Yang, R. E. Bryant, D. R. O'Hallaron, A. Biere, O. Coudert, G. Janssen, R. K. Ranjan, and F. Somenzi. A performance study of BDD-based model checking. In G. Gopalakrishnan and P. Windley, editors, *Formal Methods in Computer Aided Design*, pages 255–289. Springer-Verlag, Palo Alto, CA, November 1998. LNCS 1522.

[105] I.-H. Moon, J.-Y. Jang, G. D. Hachtel, F. Somenzi, C. Pixley, and J. Yuan. Approximate reachability don't cares for CTL model checking. In *Proceedings of the International Conference on Computer-Aided Design*, pages 351–358, San Jose, CA, November 1998.

[106] F. Ferrandi, A. Macii, E. Macii, M. Poncino, R. Scarsi, and F. Somenzi. Symbolic algorithms for layout-oriented synthesis of pass transistor logic circuits. In *Proceedings of the International Conference on Computer-Aided Design*, pages 235–241, San Jose, CA, November 1998.

[107] R. K. Ranjan, V. Singhal, F. Somenzi, and R. K. Brayton. On the optimization power of retiming and resynthesis transformations. In *Proceedings of the International Conference on Computer-Aided Design*, pages 402–407, San Jose, CA, November 1998.

[108] K. Ravi, K. L. McMillan, T. R. Shiple, and F. Somenzi. Approximation and decomposition of decision diagrams. In *Proceedings of the Design Automation Conference*, pages 445–450, San Francisco, CA, June 1998.

[109] B. Kumthekar, L. Benini, E. Macii, and F. Somenzi. In-place power optimization for LUT-based FPGAs. In *Proceedings of the Design Automation Conference*, pages 718–721, San Francisco, CA, June 1998.

[110] F. Ferrandi, A. Macii, E. Macii, M. Poncino, R. Scarsi, and F. Somenzi. Layout-oriented synthesis of PTL circuits based on BDDs. Presented at IWLS98, Lake Tahoe, CA, June 1998.

[111] B. Kumthekar, E. Macii, M. Poncino, and F. Somenzi. Simulation-based re-synthesis of sequential circuits for peak sustainable power reduction. Presented at IWLS98, Lake Tahoe, CA, June 1998.

[112] F. Somenzi, C. N. Ip, P. C. McGeer, K. L. McMillan, and K. Ravi. Combining simulation and formal verification. In *Proceedings of Cadence Technical Conference*, pages 138–142, San Antonio, TX, May 1998.

[113] J. A. Rowson, M. J. Meyer, P. C. McGeer, and F. Somenzi. Testing IP-based designs through test compression. In *Proceedings of Cadence Technical Conference*, pages 312–316, San Antonio, TX, May 1998.

[114] C. Meinel, F. Somenzi, and T. Theobald. Function decomposition and synthesis using linear sifting. In *In Proceedings of the Asia and South Pacific Design Automation Conference*, Yokohama, Japan, February 1998.

[115] E. Macii, B. F. Plessier, and F. Somenzi. Formal verification of digital systems by automatic reduction of data paths. *IEEE Transactions on Computer-Aided Design*, 16(10):1136–1156, October 1997.

[116] R. I. Bahar, H. Cho, G. D. Hachtel, E. Macii, and F. Somenzi. Symbolic timing analysis and re-synthesis for low power of combinational circuits containing false paths. *IEEE Transactions on Computer-Aided Design*, 16(10):1101–1115, October 1997.

[117] R. I. Bahar, E. A. Frohm, C. M. Gaona, G. D. Hachtel, E. Macii, A. Pardo, and F. Somenzi. Algebraic decision diagrams and their applications. *Formal Methods in Systems Design*, 10(2/3):171–206, 1997.

[118] G. D. Hachtel and F. Somenzi. A symbolic algorithm for maximum flow in 0-1 networks. *Formal Methods in Systems Design*, 10(2/3):207–219, 1997.

[119] B. Kumthekar, I.-H. Moon, and F. Somenzi. A symbolic algorithm for low-power sequential synthesis. In *International Symposium on Low Power Electronic Design*, pages 56–61, Monterey, CA, August 1997.

[120] C. Meinel, F. Somenzi, and T. Theobald. Linear sifting of decision diagrams. In *Proceedings of the Design Automation Conference*, pages 202–207, Anaheim, CA, June 1997.

[121] S. Manne, D. C. Grunwald, and F. Somenzi. Remembrance of things past: Locality and memory in BDDs. In *Proceedings of the Design Automation Conference*, pages 196–201, Anaheim, CA, June 1997.

[122] E. Macii, M. Pedram, and F. Somenzi. High-level power modeling, estimation, and optimization. In *Proceedings of the Design Automation Conference*, pages 504–511, Anaheim, CA, June 1997.

[123] M. Escobar and F. Somenzi. Projective solutions to boolean equations and the boolean matching problem. Presented at IWLS97, Lake Tahoe, CA, May 1997.

[124] B. Kumthekar, I.-H. Moon, and F. Somenzi. A symbolic algorithm for low-power sequential synthesis. Presented at IWLS97, Lake Tahoe, CA, May 1997.

[125] G. D. Hachtel and F. Somenzi. *Logic Synthesis and Verification Algorithms*. Kluwer Academic Publishers, Boston, MA, 1996.

[126] H. Cho, G. D. Hachtel, E. Macii, M. Poncino, and F. Somenzi. Automatic state space decomposition for approximate FSM traversal based on circuit analysis. *IEEE Transactions on Computer-Aided Design*, 15(12):1451–1464, December 1996.

[127] H. Cho, G. D. Hachtel, E. Macii, B. Plessier, and F. Somenzi. Algorithms for approximate FSM traversal based on state space decomposition. *IEEE Transactions on Computer-Aided Design*, 15(12):1465–1478, December 1996.

[128] G. D. Hachtel, E. Macii, A. Pardo, and F. Somenzi. Markovian analysis of large finite state machines. *IEEE Transactions on Computer-Aided Design*, 15(12):1479–1493, December 1996.

[129] W. Lee, A. Pardo, J. Jang, G. Hachtel, and F. Somenzi. Tearing based abstraction for CTL model checking. In *Proceedings of the International Conference on Computer-Aided Design*, pages 76–81, San Jose, CA, November 1996.

[130] K. Ravi, A. Pardo, G. D. Hachtel, and F. Somenzi. Modular verification of multipliers. In *Formal Methods in Computer Aided Design*, pages 49–63. Springer Verlag, Berlin, November 1996. LNCS 1166.

[131] C. Meinel, F. Somenzi, and T. Theobald. Linear sifting of decision diagrams. Technical Report 96-42, University of Trier, 1996.

[132] R. I. Bahar, M. Burns, G. D. Hachtel, E. Macii, H. Shin, and F. Somenzi. Symbolic computation of logic implications for technology-dependent low-power synthesis. In *International Symposium on Low Power Electronic Design*, pages 163–168, Monterey, CA, August 1996.

[133] F. Somenzi. Sintesi automatica di circuiti digitali. *Alta Frequenza*, 8(3), May-June 1996.

[134] S. Panda and F. Somenzi. Who are the variables in your neighborhood. In *Proceedings of the International Conference on Computer-Aided Design*, pages 74–77, San Jose, CA, November 1995.

[135] K. Ravi and F. Somenzi. High-density reachability analysis. In *Proceedings of the International Conference on Computer-Aided Design*, pages 154–158, San Jose, CA, November 1995.

[136] R. I. Bahar and F. Somenzi. Boolean techniques for low power driven resynthesis. In *Proceedings of the International Conference on Computer-Aided Design*, pages 428–432, San Jose, CA, November 1995.

[137] M. Escobar and F. Somenzi. Synthesis of AND-EXOR expressions via satisfiability. In *IFIP Workshop on the Reed-Muller Expansion in Circuit Design*, Makuhari, Chiba, Japan, August 1995.

[138] F. Somenzi and G. D. Hachtel. Symbolic graph algorithms. In *IFIP Workshop on the Reed-Muller Expansion in Circuit Design*, Makuhari, Chiba, Japan, August 1995.

[139] S. Manne, A. Pardo, R. I. Bahar, G. D. Hachtel, and F. Somenzi. Computing the maximum power cycles of a sequential circuit. In *Proceedings of the Design Automation Conference*, pages 23–28, San Francisco, CA, June 1995.

[140] H. Cho, G. D. Hachtel, E. Macii, M. Poncino, K. Ravi, and F. Somenzi. Approximate finite state machine traversal: Extensions and new results. Presented at IWLS95, Lake Tahoe, CA, May 1995.

[141] S. Panda and F. Somenzi. Who are the variables in your neighborhood. Presented at IWLS95, Lake Tahoe, CA, May 1995.

[142] M. Escobar and F. Somenzi. Synthesis of AND-EXOR expressions via satisfiability. Presented at IWLS95, Lake Tahoe, CA, May 1995.

[143] H. Shin and F. Somenzi. An exact algorithm for FPGA rectification. Presented at IWLS95, Lake Tahoe, CA, May 1995.

[144] A. Pardo, R. I. Bahar, S. Manne, P. Feldmann, G. Hachtel, and F. Somenzi. CMOS dynamic power estimation based on collapsible current source transistor modeling. In *International Symposium on Low Power Design*, pages 111–115, Dana Point, CA, April 1995.

[145] G. D. Hachtel, M. Hermida, A. Pardo, M. Poncino, and F. Somenzi. Re-encoding sequential circuits to reduce power dissipation. In *Proceedings of the International Conference on Computer-Aided Design*, pages 70–73, San Jose, CA, November 1994.

[146] R. I. Bahar, G. D. Hachtel, E. Macii, and F. Somenzi. A symbolic method to reduce power consumption of circuits containing false paths. In *Proceedings of the International Conference on Computer-Aided Design*, pages 368–371, San Jose, CA, November 1994.

[147] S. Panda, F. Somenzi, and B. F. Plessier. Symmetry detection and dynamic variable ordering of decision diagrams. In *Proceedings of the International Conference on Computer-Aided Design*, pages 628–631, San Jose, CA, November 1994.

[148] H. Cho, G. D. Hachtel, E. Macii, M. Poncino, and F. Somenzi. A structural approach to state space decomposition for approximate reachability analysis. In *Proceedings of the International Conference on Computer Design*, pages 236–239, Cambridge, MA, October 1994.

[149] J.-K. Rho and F. Somenzi. Don't care sequences and the optimization of interacting finite state machines. *IEEE Transactions on Computer-Aided Design*, 13(7):865–874, July 1994.

[150] G. D. Hachtel, E. Macii, A. Pardo, and F. Somenzi. Probabilistic analysis of large finite state machines. In *Proceedings of the Design Automation Conference*, pages 270–275, San Diego, CA, June 1994.

[151] R. I. Bahar, H. Cho, G. D. Hachtel, E. Macii, and F. Somenzi. An application of ADD-based timing analysis to combinational low power resynthesis. Presented at the International Workshop on Low Power Design, Napa, CA, April 1994.

[152] G. D. Hachtel, M. Hermida, A. Pardo, M. Poncino, and F. Somenzi. Reencoding sequential circuits to reduce power dissipation. Presented at the International Workshop on Low Power Design, Napa, CA, April 1994.

[153] R. I. Bahar, G. D. Hachtel, E. Macii, A. Pardo, M. Poncino, and F. Somenzi. An ADD-based algorithm for shortest path back-tracing of large graphs. In *VLSI Great Lakes Symposium*, pages 248–251, University of Notre Dame, IN, March 1994.

[154] B. Plessier, G. Hachtel, and F. Somenzi. Extended BDDs: Trading off canonicity for structure in verification algorithms. *Formal Methods in System Design*, 4(2):167–185, February 1994.

[155] J.-K. Rho, G. D. Hachtel, F. Somenzi, and R. Jacoby. Exact and heuristic algorithms for the minimization of incompletely specified state machines. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 13(2):167–177, February 1994.

[156] R. I. Bahar, H. Cho, G. D. Hachtel, E. Macii, and F. Somenzi. Timing analysis of combinational circuits using ADD's. In *Proceedings of the European Conference on Design Automation*, pages 625–629, Paris, France, February 1994.

[157] G. D. Hachtel, E. Macii, A. Pardo, and F. Somenzi. Symbolic algorithms to calculate steady-state probabilities of a finite state machine. In *Proceedings of the European Conference on Design Automation*, pages 214–218, Paris, France, February 1994.

[158] H. Cho, G. D. Hachtel, E. Macii, M. Poncino, and F. Somenzi. A state space decomposition algorithm for approximate FSM traversal. In *Proceedings of the European Conference on Design Automation*, pages 137–141, Paris, France, February 1994.

[159] R. I. Bahar, E. A. Frohm, C. M. Gaona, G. D. Hachtel, E. Macii, A. Pardo, and F. Somenzi. Algebraic decision diagrams and their applications. In *Proceedings of the International Conference on Computer-Aided Design*, pages 188–191, Santa Clara, CA, November 1993.

[160] G. D. Hachtel and F. Somenzi. A symbolic algorithm for maximum flow in 0-1 networks. In *Proceedings of the International Conference on Computer-Aided Design*, pages 403–406, Santa Clara, CA, November 1993.

[161] S.-W. Jeong, T.-S. Kim, and F. Somenzi. An efficient method for optimal BDD ordering computation. In *International Conference on VLSI and CAD (ICVC'93)*, Taejon, Korea, November 1993.

[162] H. Cho, G. D. Hachtel, and F. Somenzi. Redundancy identification/removal and test generation for sequential circuits using implicit state enumeration. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 12(7):935–945, July 1993.

[163] J.-K. Rho and F. Somenzi. Automatic generation of network invariants for the verification of iterative sequential systems. In C. Courcoubetis, editor, *Fifth Conference on Computer Aided Verification (CAV '93)*, pages 123–137. Springer-Verlag, Berlin, 1993. LNCS 697.

[164] J.-K. Rho, F. Somenzi, and C. Pixley. Minimum length synchronizing sequences of finite state machines. In *Proceedings of the Design Automation Conference*, pages 463–468, Dallas, TX, June 1993.

[165] H. Cho, G. D. Hachtel, E. Macii, B. Plessier, and F. Somenzi. Algorithms for approximate FSM traversal based on state space decomposition. In *Proceedings of the Design Automation Conference*, pages 25–30, Dallas, TX, June 1993.

[166] G. D. Hachtel and F. Somenzi. A symbolic algorithm for maximum flow in 0-1 networks. Presented at IWLS'93, May 1993.

[167] H. Cho, S.-W. Jeong, F. Somenzi, and C. Pixley. Synchronizing sequences and symbolic traversal techniques in test generation. *Journal of Electronic Testing: Theory and Aplications*, 4:19–31, 1993.

[168] H. Cho and F. Somenzi. Sequential logic optimization based on state space decomposition. In *Proceedings of the European Conference on Design Automation*, pages 200–204, Paris, France, February 1993.

[169] H. Cho, S.-W. Jeong, F. Somenzi, and C. Pixley. Multiple observation time single reference test generation using synchronizing sequences. In *Proceedings of the European Conference on Design Automation*, pages 494–498, Paris, France, February 1993.

[170] S.-W. Jeong and F. Somenzi. A new algorithm for 0-1 programming based on binary decision diagrams. In T. Sasao, editor, *Logic Synthesis and Optimization*, chapter 7, pages 145–165. Kluwer Academic Publishers, Boston, MA, 1993.

[171] E. Macii, B. Plessier, and F. Somenzi. Verification of systems containing counters. In *Proceedings of the International Conference on Computer-Aided Design*, pages 179–182, Santa Clara, CA, November 1992.

[172] S.-W. Jeong and F. Somenzi. A new algorithm for the binate covering problem and its application to the minimization of boolean relations. In *Proceedings of the International Conference on Computer-Aided Design*, pages 417–420, Santa Clara, CA, November 1992.

[173] J.-K. Rho and F. Somenzi. The role of prime compatibles in the minimization of finite state machines. In *Proceedings of the International Conference on Computer Design*, pages 324–327, Boston, MA, October 1992.

[174] S.-W. Jeong and F. Somenzi. A new algorithm for 0-1 programming based on binary decision diagrams. In *International Symposia on Information Sciences*, pages 177–184, Iizuka, Fukuoka, Japan, July 1992. Kyushu Institute of Technology.

[175] J.-K. Rho and F. Somenzi. Inductive verification for iterative systems. In *Proceedings of the Design Automation Conference*, pages 628–633, Anaheim, CA, June 1992.

[176] Q. Ji, Y.-S. Oh, M. R. Lightner, and F. Somenzi. Technology independent estimation of area and delay in logic synthesis. In *SASIMI '92*, pages 171–180, Kyoto, Japan, April 1992.

[177] S.-W. Jeong, B. F. Plessier, G. D. Hachtel, and F. Somenzi. Variable ordering for binary decision diagrams. In *Proceedings of the European Conference on Design Automation*, pages 447–451, Brussels, March 1992.

[178] J.-K. Rho, G. D. Hachtel, and F. Somenzi. Don't care sequences and the optimization of interacting finite state machines. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 418–421, Santa Clara, CA, November 1991.

[179] S.-W. Jeong, B. Plessier, G. D. Hachtel, and F. Somenzi. Extended BDD's: Trading off canonicity for structure in verification algorithms. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 464–467, Santa Clara, CA, November 1991.

[180] S.-W. Jeong, B. Plessier, G. D. Hachtel, and F. Somenzi. Variable ordering and selection for FSM traversal. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 476–479, Santa Clara, CA, November 1991.

[181] H. Cho, G. D. Hachtel, and F. Somenzi. Redundancy identification and removal based on implicit state enumeration. In *Proceedings of the International Conference on Computer Design*, pages 77–80, Cambridge, MA, October 1991.

[182] H. Cho, G. D. Hachtel, and F. Somenzi. Fast sequential ATPG based on implicit state enumeration. In *Proceedings of the International Test Conference*, pages 67–74, Nashville, TN, October 1991.

[183] J.-K. Rho, G. D. Hachtel, and F. Somenzi. Don't care sequences and the optimization of interacting finite state machines. In *Proceedings of the International Workshop on Logic Synthesis*, MCNC, Research Triangle Park, NC, May 1991.

[184] H. Cho, G. D. Hachtel, and F. Somenzi. Redundancy identification and removal based on BDD's and implicit state enumeration. In *Proceedings of the International Workshop on Logic Synthesis*, MCNC, Research Triangle Park, NC, May 1991.

[185] S.-W. Jeong, B. Plessier, G. D. Hachtel, and F. Somenzi. Variable ordering for FSM traversal. In *Proceedings of the International Workshop on Logic Synthesis*, MCNC, Research Triangle Park, NC, May 1991.

[186] M. Favalli, P. Olivo, B. Riccò, and F. Somenzi. Fault simulation for general FCMOS ICs. *Journal of Electronic Testing: Theory and Applications*, 2(2):181–190, May 1991.

[187] H. Cho, G. D. Hachtel, and F. Somenzi. Sequential logic optimization by testing techniques. In *RockCon '91 – ASTE Regional Test Conference*, Denver, CO, May 1991.

[188] G. D. Hachtel, J.-K. Rho, F. Somenzi, and R. Jacoby. Exact and heuristic algorithms for the minimization of incompletely specified state machines. In *Proceedings of the European Design Automation Conference*, pages 184–191, Amsterdam, The Netherlands, February 1991.

[189] T. L. Weber and F. Somenzi. Periodic signal suppression in a concurrent fault simulator. In *Proceedings of the IEEE European Conference on Design Automation*, pages 565–569, Amsterdam, The Netherlands, February 1991.

[190] H. Cho, G. D. Hachtel, S.-W. Jeong, B. Plessier, E. Schwarz, and F. Somenzi. Results on the interface between formal verification and ATPG. In E. M. Clarke and R. P. Kurshan, editors, *Computer-Aided Verification '90*, pages 615–628. American Mathematical Society – Association for Computing Machinery, 1991.

[191] B. Lin and F. Somenzi. Minimization of symbolic relations. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 88–91, Santa Clara, CA, November 1990.

[192] H. Cho, G. D. Hachtel, S.-W. Jeong, B. Plessier, E. Schwarz, and F. Somenzi. ATPG aspects of FSM verification. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 134–137, November 1990.

[193] M. Pipponzi and F. Somenzi. An iterative approach to the binate covering problem. In *Proceedings of the European Conference on Design Automation*, pages 208–211, Glasgow, UK, March 1990.

[194] R. K. Brayton and F. Somenzi. An exact minimizer for Boolean relations. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 316–319, Santa Clara, CA, November 1989.

[195] I. Causarano, R. Guizzetti, M. Pipponzi, and F. Somenzi. MSYN: Automatic synthesis of hardware. *Microprocessing and Microprogramming*, 27:367–372, September 1989.

[196] R. K. Brayton and F. Somenzi. Boolean relations and the incomplete specification of logic networks. In G. Musgrave and U. Lauther, editors, *VLSI '89*, pages 231–240. North-Holland, Amsterdam, 1989.

[197] R. Brayton and F. Somenzi. Minimization of boolean relations. In *Proc. Int. Symp. Circ. Syst. (ISCAS-89)*, pages 738–743, Portland, OR, May 1989.

[198] R. K. Brayton and F. Somenzi. Boolean relations. In *International Workshop on Logic Synthesis*, May 1989.

[199] R. Brayton, E. Sentovich, and F. Somenzi. Don't-cares and global flow analysis of boolean networks. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 98–101, Santa Clara, CA, November 1988.

[200] S. Gai, P. L. Montessoro, and F. Somenzi. MOZART: A concurrent multilevel simulator. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 7:1005–1016, September 1988.

[201] G. P. Cabodi, S. Gai, M. Mezzalama, P. L. Montessoro, and F. Somenzi. Fault simulation in a multilevel environment: The MOZART approach. In *Proceedings of the IEEE International Fault Tolerant Computing Symposium*, pages 128–133, Tokyo, Japan, June 1988.

[202] S. Gai, P. L. Montessoro, and F. Somenzi. The performance of the concurrent fault simulation algorithms in MOZART. In *Design Automation Conference*, pages 692–697, Anaheim, CA, June 1988.

[203] S. Gai, F. Somenzi, and E. Ulrich. Advances in concurrent multilevel simulation. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, CAD-6:1006–1012, November 1987.

[204] S. Gai, F. Somenzi, and M. Spalla. Fast and coherent simulation with zero delay elements. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, CAD-6:85–92, January 1987.

[205] S. Gai, F. Somenzi, and E. Ulrich. Advanced techniques for concurrent multilevel simulation. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 334–337, Santa Clara, CA, November 1986.

[206] F. Somenzi and S. Gai. Fault detection in programmable logic arrays. *Proceedings of the IEEE*, 74:655–668, May 1986.

[207] S. Gai, F. Somenzi, and M. Spalla. Zero delay elements in logic simulation. In *Communication to Euromicro 85*, Brussels, Belgium, September 1985.

[208] F. Somenzi, S. Gai, M. Mezzalama, and P. Prinetto. Testable design with PLA macros. *Microprocessing and Microprogramming*, 15:119–128, March 1985.

[209] F. Somenzi, S. Gai, M. Mezzalama, and P. Prinetto. Testing strategy and technique for macro-based circuits. *IEEE Transactions on Computers*, C-34:85–90, January 1985.

[210] A. Poretta, M. Santomauro, and F. Somenzi. TAU: A fast heuristic logic minimizer. In *Proceedings of the IEEE International Conference on Computer Aided Design*, pages 206–208, Santa Clara, CA, November 1984.

[211] A. Lioy, M. Mezzalama, and F. Somenzi. Efficient testability measures for NMOS-LSI circuits. In *Proceedings of the 24th International Symposium on Mini and Micro Computers and Their Applications (MIMI'84)*, Bari, Italy, June 1984.

[212] F. Somenzi, S. Gai, M. Mezzalama, and P. Prinetto. PART: Programmable ARray Testing based on a PARTitioning algorithm. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, CAD-3(2):142–149, April 1984.

[213] S. Gai, M. Mezzalama, P. Prinetto, and F. Somenzi. ART*: A register transfer level simulation system. In *Proceedings of the IEEE International Conference on Computer Aided Design*, page 151, Santa Clara, CA, September 1983.

[214] F. Somenzi, S. Gai, M. Mezzalama, and P. Prinetto. Testable design with PLA macros. In F. Anceau and E. J. Aas, editors, *VLSI '83*, pages 373–382. North-Holland, Amsterdam, 1983.

[215] F. Somenzi, S. Gai, M. Mezzalama, and P. Prinetto. PART: Programmable ARray Testing based on a PARTitioning algorithm. In *Proceedings of the IEEE International Fault Tolerant Computing Symposium*, pages 430–433, Milano, Italy, June 1983.

[216] F. Somenzi, S. Gai, M. Mezzalama, and P. Prinetto. A new integrated system for PLA testing and verification. In *Proceedings of the Design Automation Conference*, pages 57–63, Miami Beach, FL, June 1983.

[217] S. Gai, M. Mezzalama, P. Prinetto, and F. Somenzi. Programmable array logic simulation in a RTL environment. In *Proceedings of the IEEE Mediterranean Electrotechnical Conference (Melecon)*, Athens, Greece, May 1983.

[218] F. Somenzi, S. Gai, M. Mezzalama, and P. Prinetto. PART: Programmable ARray Testing based on a PARTitioning algorithm. In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pages 1298–1301, Newport Beach, CA, May 1983.

[219] F. Somenzi, S. Gai, M. Mezzalama, and P. Prinetto. Testing strategies for PLA based circuits. In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pages 1302–1305, Newport Beach, CA, May 1983.