Chris John Myers

Department of Electrical, Computer, and Energy Engineering, University of Colorado Boulder
Engineering Center, Room ECEE 1B55, Boulder, CO 80309
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Education

Stanford University, Stanford, California (1991-1995)

Ph.D. degree in Electrical Engineering (1995)
Thesis: Computer-Aided Synthesis and Verification of Gate-Level Timed Circuits

M.S. degree in Electrical Engineering (1993)

California Institute of Technology, Pasadena, California (1987-1991)

B.S. degree with honor in Electrical Engineering and History (1991)

Professional Experience

Chair of Elec., Comp., and Energy Eng., *University of Colorado Boulder* (2020-present)
Professor of Elec., Comp., and Energy Eng., *University of Colorado Boulder* (2020-present)
Affiliated Professor of Biomedical Engineering, *University of Colorado Boulder* (2020-present)
Affiliated Professor of Computer Science, *University of Colorado Boulder* (2020-present)
Adjunct Professor of Electrical and Computer Eng., *University of Utah* (2021-2024)
Adjunct Professor of Computer Science, *University of Utah* (2007-2024)
Adjunct Professor of Bioengineering, *University of Utah* (2007-2024)
Professor of Electrical and Computer Engineering, *University of Utah* (2006-2021)
Associate Chair of Electrical and Computer Engineering, *University of Utah* (2018-2020)
Visiting Professor of Engineering Science, *University of Oxford* (summer 2019)
Visiting Professor of Electrical and Computer Engineering, *Boston University* (2017)
Visiting Professor of Computer Science, *Newcastle University* (2016-2017)
Director of Computer Engineering, *University of Utah* (2000-2002, 2006-2009)
Adjunct Associate Professor of Computer Science, *University of Utah* (2003-2007)
Adjunct Associate Professor of Bioengineering, *University of Utah* (2003-2007)
Associate Professor of Electrical and Computer Eng., *University of Utah* (2001-2006)
Visiting Scholar, *Tokyo Institute of Technology* (summer 2003)
Visiting Scholar, *Stanford University* (2002-2003)
Research Assistant Professor of Computer Science, *University of Utah* (1996-2003)
Director of the Center for Asynchronous Circuit Design, *University of Utah* (1997-2001)
Assistant Professor of Electrical Engineering, *University of Utah* (1995-2001)
Consultant, Intel Corporation, Portland, Oregon, (1996-1998)
Consultant, Intel Corporation, Haifa, Israel, (summer 1995)
Research Assistant, Professor Teresa Meng, *Stanford University* (1991-1995)
Teaching Assistant, Professor Charles Seitz, *California Institute of Technology* (1990-1991)
Research Assistant, Professor James Lee, *California Institute of Technology* (1989-1991)
Software Engineer, Business Data Systems, Billings, Montana (1985-1989)

Awards

Deans Research and Policy Advancement Fellow, *University of Colorado Boulder* (2025)
CEAS Textbook Recognition Award, *University of Colorado Boulder* (2024)
Fellow of the IEEE (2013)
ECE Departmental Service Award, *University of Utah* (2013)
Best Paper Award, Symposium on Asynchronous Circuits and Systems (2007)
Best Paper Award Finalist, Symposium on Asynchronous Circuits and Systems (2001)
Best Paper Award, Symposium Asynchronous Circuits and Systems (1999)
Teaching commendation for CS/EE 5740, *University of Utah* (1998)
National Science Foundation CAREER Award (1996)
National Science Foundation Graduate Fellowship (1991)
Rodman W. Paul History Prize, *California Institute of Technology* (1991)
Tau Beta Pi National Honor Society (1991)
Carnation Merit Award, *California Institute of Technology* (1990)
First Prize VLSI Design Contest, *California Institute of Technology* (1990)

Grant Activities

1. C. Myers, "EBUGS (Engineering Biology for Underwater and Ground Sensors)", May 2024 - October, 2026, DARPA (sub-award from Draper), $538,242.
2. C. Myers, "CHARMME: Center for Harnessing Microbiota from Military Environments", September 2022 - September 2027, Army Research Organization (sub-award from MIT) $750,000.
3. C. Myers, "SynBioHub3 - An Interactive Genetic Design Repository", October 2021 - September 2024, National Institute of Standards and Technology, $179,975.
4. C. Myers, "EAGER: Accelerating Synthetic Biology Discovery through Integrated Curation", August 2022 - July 2025, National Science Foundation, $300,000.
5. C. Myers, "An Efficient Framework for the Stochastic Verification of Computation and Communication Systems Using Emerging Technologies", July 2019 - December 2024, National Science Foundation, $346,000.
6. C. Myers, "Accelerating Synthetic Biology Discovery & Exploration through Knowledge Integration", October 2019 - September 2022, National Science Foundation, $204,296.
7. C. Myers, "Genetic circuit design for extreme environments enabled by models extracted from petabyte+ perturbation analyses", July 2018 - March 2022, DARPA, $308,353.
8. C. Myers, "NSF Student Travel Grant for 2018 Computational Modeling in Biology Network (COMBINE) Forum", May 2018 - May 2019, National Science Foundation, $10,000.
9. C. Myers, "NSF Student Travel Grant for 2018 Hackathons on Resources for Modeling in Biology (HARMONY)", May 2018 - May 2019, National Science Foundation, $10,000.
10. C. Myers, "Evolvable Living Computing - Understanding and Quantifying Synthetic Biological Systems' Applicability, Performance, and Limits", August 2017 - August 2018, National Science Foundation (sub-award from Boston University), $41,266.
11. C. Myers, "A Standard Enabled Workflow for Synthetic Biology", August 2017 - August 2019, National Science Foundation, $150,000, REU supplements totaling $31,758.
12. C. Myers, "Student Travel Support for COMBINE 2016", June 2016 - May 2017, National Science Foundation, $15,000.
13. C. Myers, "Student Travel Support for SBOL 14 Workshop", March 2016 - March 2017, National Science Foundation, $10,000.

14. C. Myers, "Student Travel Support for COMBINE 2015", June 2015 - May 2016, National Science Foundation, two awards totally $16,000.
15. C. Myers, H. Sauro (UW), and J. Gennari (UW), "Synthetic Biology Open Language Resource", July 2014 - June 2018, National Science Foundation, $444,527 (Utah share).
16. C. Myers, "Student Travel Support for HARMONY 2015", July 2014 - June 2015, National Science Foundation, $10,000.
17. C. Myers, "Genetic Design Automation", July 2012 - June 2015, National Science Foundation, $449,980, REU supplements totaling $32,000, travel supplement $15,000.
18. C. Myers and P. Li (TAMU), "Integrated Verification, Built-in Self-test, and Tuning for Digitally-Intensive Analog Systems", July 2011 - July 2014, Nat. Sci. Foundation, $224,998 (Utah share).
19. C. Myers, "Simulation Aided Verification of AMS Circuits", May 2010 - January 2011, Intel Corporation, $35,000.
20. C. Myers and H. Zheng (USF), "Methods and Tools for the Verification of Cyber-Physical Systems", September 2009 - August 2012, National Science Foundation, $270,000 (Utah share).
21. C. Myers and C. Winstead (USU), "Soft-Logic Modeling and Design for Synthetic Biology", July 2009 - June 2012, National Science Foundation, $262,000 (Utah share).
22. C. Myers, "Simulation Aided Verification of AMS Circuits", October 2008 - September 2011, Semiconductor Research Corporation, $198,864.
23. C. Myers, "Designing Reliable Systems Using Unreliable Components", July 2007 - June 2009, National Science Foundation, $150,000.
24. C. Myers, "Formal Verification of Analog and Mixed-Signal Circuits", October 2005 - September 2008, Semiconductor Research Corporation, $270,000.
25. C. Myers, "A Principled Mapping of Regulatory Networks to Asynchronous Circuit Models for Stochastic Analysis", September 2003 - August 2006, National Science Foundation, $425,864, REU supplement $5,000.
26. C. Myers, "System-Level Timing Verification with Automatic Abstraction", August 2002 - July 2005, Semiconductor Research Corporation, $270,000.
27. C. Myers, "U.S.-Japan Cooperative Science: Synthesis and Verification of High Performance Timed Circuits and Systems", April 2001 - April 2004, National Science Foundation, $30,000.
28. C. Myers, C. Schlegel (co-PI), R. Harrison (co-PI), "Design Methodology for Mixed Analog/Asynchronous VLSI Implementations of Communications Systems", September 1999 - August 2002, National Science Foundation, $300,000, REU supplement $5,000.
29. C. Myers, "Timing Verification using Automatic Abstraction", July 1999 - June 2002, Semiconductor Research Corporation, $174,000.
30. C. Myers, E. Brunvand (co-PI), "Center for Asynchronous Circuit and System Design", July 1999 - June 2000, State of Utah, $130,000.
31. C. Myers, "Synthesis and Verification of Timed Circuits", August 1997 - July 2000, Semiconductor Research Corporation, $150,000.
32. C. Myers, "Specification and Compilation Techniques for 1 GHz and Beyond", awarded May 1998, Intel Corporation, $20,000.
33. C. Myers, E. Brunvand (co-PI), "Center for Asynchronous Circuit and System Design", July 1998 - June 1999, State of Utah, $115,000.
34. C. Myers, E. Brunvand (co-PI), "Center for Asynchronous Circuit and System Design", July 1997 - June 1998, State of Utah, $100,000.
35. C. Myers, "Design Methods and Tools for Mixed-Timed Systems", July 1996 - June 2000, NSF CAREER Award, $210,000, U. of Utah matching grant $5,000, REU supplement $5,000.

Development Activities

1. Cash gift from Intel Corporation for research, Dec 2011, $28,000.
2. Cash gift from CEDA to support FAC workshop, June 2011, $3,000.
3. Cash gift from Intel to support FAC workshop, Dec 2010, $2,000.
4. Cash gift from SRC to support verification review, Dec 2006, $5,000.
5. Several cash gifts from SRC to support undergraduate research, May 2006, $6,000, Sept. 2005, $6,000, May 2005, $6,000, Sept. 2004, $6,000, May 2004, $6,000, May 2003, $12,000, Sept. 2002, $12,000, May 2002, $6,000, Aug. 2001, $18,000, May 2001, $12,000, Oct. 2000, $6,000.
6. Cash gift from SRC to support verification review, Dec 2001, $5,000.
7. Computer equipment donation from Intel Corporation, October 2000, valued at $20,000.
8. Software donation from VeriBest Incorporated, January 1999, valued at $2,250,000.
9. Cash gift from Intel Corporation for research, June 1997, $20,000.
10. Software donation from Intel Corporation, July 1996, valued at $1,100.
11. Cash gift from Intel Corporation for research, April 1996, $53,600.
12. Computer equipment donation from Intel Corporation, March 1996, valued at $12,756.
13. Cash gift from Intel Corporation for research, January 1996, $15,500.

Languages

Working knowledge of written and spoken Chinese.

Academic Service

BioFrontiers Council Member, *University of Colorado Boulder* (2020-present)
ECEE Search Committee Co-Chair, *University of Colorado Boulder* (2024-2025)
Biomedical Eng. Search Committee Co-Chair, *University of Colorado Boulder* (2023-2024)
Biomedical Eng. Search Committee Member, *University of Colorado Boulder* (2022-2023)
Computer Engineering Committee Member, *University of Utah* (1995-2016, 2018-2020)
Recruiting Committee Chairman, *University of Utah* (2001-2002, 2004-2006, 2017-2018)
Recruiting Committee Member, *University of Utah* (1995-2000, 2015-2016, 2018-2019)
Coordinator for Electrical Engineering Senior Projects, *University of Utah* (2011-2013)
Faculty Senate, *University of Utah* (2010-2013)
Computer Engineering Director, *University of Utah* (2000-2002, 2006-2009)
Organizer of Judd Distinguished Lecture Series, *University of Utah* (2005-2008)
Assessment and Planning Committee, *University of Utah* (2003-2004)
Strategic Goals Committee Member, *University of Utah* (1997-2001)
Curriculum Committee Member, *University of Utah* (1995-1998)
Computing Committee Member, *University of Utah* (1995-1998)
College Council Member, *University of Utah* (1995-1998)
Alumni Fund House Chair, *California Institute of Technology* (1994-1998)

Professional Activities

Member of the IEEE, S'91-M'96-SM'04-Fellow'13 (1991-present)

Member of the ACM (1996-present)

Member of the Organizing Committee for SEED 2026 (2025-present)

Member of the iGEM Registry Steering Committee (2026-present)

General Chair for 2026 Int. Workshop on Bio-Design Automation (2025-present)

Member of the ECEDHA Board of Directors (2024-present)

Member of the External Advisory Board for the Engineering Biology CDT, *Oxford University* (2025-present)

Chair of the External Advisory Board for the BioDesign CDT, *Imperial College London* (2019-present)

Member of the Editorial Board, *Engineering Biology* (2016-present)

Member of the Editorial Board, *Synthetic Biology* (2016-present)

Member of the Steering Committee, *Synthetic Biology Open Language* (2015-present)

Member, COmputational Modeling in Biology NEtworks Coord. Board (2014-present)

Chair of the Steering Committee, *Synthetic Biology Open Language* (2019-2023)

Co-organizer, Western ECE Department Heads Meeting, (2023)

Co-organizer, NSF Workshop on Rigorous & Reproducible Scientific Reasoning, (2023)

Int. Rep. on the SynBio CDT Directorate Comm., *Oxford University* (2016-2022)

Member of the Portabolomics Advisory Board, *Newcastle University* (2016-2022)

Member of the Organizing Committee for SEED 2022 (2021-2022)

Chair, COmputational Modeling in Biology NEtworks Coordination Board (2019-2021)

Member of the Steering Committee, *Synthetic Biology Standards Consortium* (2015-2020)

Member of the Steering Committee, *Frontiers in Analog CAD Workshop* (2010-2018)

Associate Editor, *IEEE Life Sciences Letters*, (2014-2017)

Guest Editor, *IEEE Design & Test Magazine* (2015-2016)

Organizer, *COMBINE Forum 2015* (2015)

Member of the Editorial Board, *Frontiers in Synthetic Biology* (2013-2015)

Associate Editor, *IEEE Transactions on VLSI* (2009-2014)

Member of the Editorial Board, *Formal Methods in System Design* (2006-2014)

Guest Editor, *ACM Journal of Emerging Technologies in Computing Systems*, (2013-2014)

Associate Editor, *IEEE Design and Test Magazine*, (2012-2014)

Editor, *Systems Biology Markup Language* (SBML) (2011-2013)

Guest Editor, *ACS Synthetic Biology*, (2013)

Member of the Review Panel, *NIH MABS Study Section* (2012)

Simulation and Verification Track Chair, *Int. Conf. on Computer-Aided Design* (2012)

Publications Chair, *Int. Workshop on Bio-Design Automation* (2012)

Co-Program Chair, *Frontiers in Analog CAD Workshop* (2011)

Site Reviewer, *NSF Expeditions* (2011)

Member of the Best Paper Committee, *Async. Circuits and Systems Conf.* (2006, 2008)

Organizer, *SRC Verification Review* (2002, 2007)

Co-organizer and Technical Program Chair, *Asynchronous Circuits and Systems Conf.* (2001)
Co-organizer and Technical Program Chair, *Advanced Research in VLSI Conf.* (2001)
Tools Chair, *Asynchronous Circuits and Systems Conference* (1998)
Member of the PC, *Int. Workshop on Bio-Design Automation* (2009-present)
Member of the PC, *Async Ckts/Sys Conf.* (1998-2004, 2006, 2008-2009, 2011, 2017)
Member of the PC, *Conference on Analysis and Design of Hybrid Systems* (2017)
Member of the PC, *Winter Simulation Conference* (2017)
Member of the PC, *Workshop on Hybrid Systems and Biology* (2013)
Member of the PC, *Int. Conf. on Formal Modeling and Analysis of Timed Sys.* (2010)
Member of the PC, *Frontiers in Analog CAD Workshop* (2005-2018)
Member of the PC, *ACM Int. Conf. on Nanoscale Comp. and Comm.* (2016, 2018)
Member of the PC, *IJCAI 2016 Workshop: AI for Synthetic Biology* (2015-2016)
Member of the PC, *Symposium on Theory of Modeling and Simulation* (2014-2017)
Member of the PC, *Forum on Specification and Design Languages* (2011-2016)
Member of the PC, *Workshop on Modeling of Biological Systems*, (2013)
Member of the PC, *ICNC Workshop on Cyber-Physical Systems* (2013)
Member of the PC, *ISMB SIG on Biological System Design* (2012)
Member of the PC, *Int. Conf. on Bioinfo., Biocomp. Sys., and BioTech.* (2011-2012)
Member of the PC, *Great Lakes Symposium on VLSI* (2010-2012)
Member of the PC, *Int. Conf. on Computer-Aided Design* (2009-2012)
Member of the PC, *Virtual Worldwide Forum on Electronic Design Automation*, (2011)
Member of the PC, *Logic Aspects of Fault Tolerance*, (2009, 2011)
Member of the PC, *Int. Conf. on Computational and Systems Biology* (2010)
Member of the PC, *Int. Conf. on Information Technology* (2007)
Member of the PC, *Conf. on Information Technology* (2006)
Member of the PC, *Formal Methods for GALS* (2003, 2005)
Member of the PC, *Computer Aided Verification Conference* (2003-2004)
Member of the PC, *Workshop on Theory and Practice of Timed Systems* (2002)
Panelist and Reviewer, Proposals for NSF, NIH, DOE, Chan/Zuckerberg, etc.
Reviewer, *Morgan Kaufman, McGraw Hill, Wiley, ACS Synthetic Biology, Nature, and many IEEE journals*

Graduated Students (Committee Chairman)

PhD - Lukas Buecherl - Decoding Genetic Circuit Failures, 5/24.
PhD - Pedro Fontanarrosa - Auto. Gen. of Dynamic Models for Genetic Regulatory Net., 8/22.
PhD - Jeanet Mante - Promotion of Data Reuse in Synthetic Biology, 5/22.
PhD - Tramy Nguyen - Asynchronous Genetic Circuit Design, 9/19.
PhD - Leandro Watanabe - Modeling and Simulation for Heterogeneous Populations, 12/18.
PhD - Zhen Zhang - Verification Methodologies for Fault-Tolerant NoC Systems, 12/15.
PhD - Andrew Fisher - Efficient, Sound Formal Verification for AMS Circuits, 8/15.
PhD - Nicholas Roehner - Technology Mapping of Genetic Circuit Designs, 8/14.
PhD - Curtis Madsen - Stochastic Analysis of Synthetic Genetic Circuits, 8/13.
PhD - Robert Thacker - A New Verification Method For Embedded Systems, 12/10.
PhD - Scott Little - Efficient Modeling and Verif. of AMS Circuits Using LHPNs, 8/08.
PhD - Nathan Barker - Learning Genetic Reg. Net. Connectivity from Time Series Data, 8/07.
PhD - Hiroyuki Kuwahara - Model Abs. & Temp. Behv. Analysis of Genetic Reg. Net., 8/07.
PhD - David Walter - Verification of AMS Circuits Using Symbolic Methods, 8/07.
PhD - Curt Nelson - Technology Mapping of Timed Cirucits, 12/04.
PhD - Hans Jacobson - Interlocked Synchronous Pipelines, 12/03.
PhD - Eric Mercer - Correctness and Reduction in Timed Circuit Analysis, 12/02.
PhD - Jie Dai - Design Methodology for Analog VLSI Impl. of Error Control Decoders, 12/02.
PhD - Eric Peskin - Protocol Selection, Impl., and Analysis for Asynchronous Circuits, 8/02.
PhD - Hao Zheng - Modular Syn.&Verif. of Timed Circuits Using Automatic Abstraction, 8/01.
PhD - Wendy Belluomini - Algorithms for Synthesis and Verification of Timed Circuits, 9/99.
MS - Logan Terry, SBOLCanvas: A Visual Editor for Genetic Designs, 5/21.
MS - Pedro Fontanarrosa, Automated Generation of Dynamic Models for GRNs, 6/19.
MS - Michael Zhang, SBOLExplorer: Data Mining for Genetic Design Repositories, 4/19.
MS - Meher Samineni, Software Compliance Testing for Workflows using SBOL, 8/18.
MS - Dhanashree Kulkarni, Improved Model Gen. and Prop. Spec. for AMS Circuits, 8/13.
MS - Satish Batchu - Automatic Extraction of Behv. Models from Sim. of AMS Circuits, 12/10.
MS - Nam Nguyen - Design and Analysis of Genetic Circuits, 8/08.
MS - Yanyi Zhao - Application of Sync Synthesis Tools for High-Level Async Design, 12/04.
MS - Chris Krieger - Complete State Coding of Timed Asynchronous Circuits, 12/02.
MS - Kip Killpack - Analysis and Characterization of a Locally-Clocked Module, 5/02.
MS - Robert Thacker - Implicit Methods for Timed Circuit Synthesis, 6/98.
MS - Hao Zheng - Specification and Compilation of Timed Systems, 6/98.
MS - Brandon Bachman - Architectural-Level Synthesis for Asynchronous Systems, 9/98.
MS - Eric Mercer - Stochastic Cycle Period Analysis in Timed Circuits, 5/99.
BS - Eric Yu, SynBioHub3 Back-End, 5/22.
BS - Michael Zhang, SBOLDesigner: A Hierarchical Genetic Design Editor, 4/18.
BS - Meher Samineni, Software Compliance Testing for SBOL, 8/17.
BS - Leandro Watanabe - Hierarchical Stochastic Simulation Algorithm, 5/14.

BS - Tyler Patterson - Modeling and Visualization of Genetic Circuits, 5/11.
BS - Kevin Jones - Automated Abstraction of Labeled Petri Nets, 5/11.
BS - Scott Little - Comparative Study of Several Timing Analysis Algorithms, 5/03.
BS - Yanyi Zhao - An Aysnchronous MPEG Ditherer, 5/03.
BS - Allen Sjogren - Interfacing Synchronous and Asynchronous Modules, 5/98.
BS - Jeff Cuthbert - XATACS: The Next Generation in Asynchronous Circuit Design, 5/98.

Current Graduate Students (Committee Chairman)

PhD - Daniel Fang, Computer Science, University of Colorado Boulder
PhD - Chunxiao Liao, Computer Science, University of Colorado Boulder
PhD - William Mo, Biomedical Engineering, University of Colorado Boulder
PhD - Hatem Mohamed, Biomedical Engineering, University of Colorado Boulder
PhD - Carolus Vitalis, Biomedical Engineering, University of Colorado Boulder
MS - Zane Perry, Applied Mathematics, University of Colorado Boulder

Postdocs Supervised

Gonzalo Vidal Pena - Data Management for Synthetic Biology (2023-present)
Pedro Fontanarrosa - Characterization and Modeling of Genetic Parts (2022-2023)
Jeanet Mante - Integrated Curation for Synthetic Biology (2022-2023)
Zhen Zhang - libSBOLj: A Java Library for SBOL (2015-2016)
Jian Wu - Analysis of Network-on-Chip Routing Protocols (2010-2011)
Sung-tae Jung - Direct Synthesis of Timed Circuits (1999-2000)

Undergraduate Projects Supervised

Saanika Fadia - SynBioSuite Server (2025-present)
Conner Groth - SeqImprove2 (2025-present)
Indiana Kretzschmar - Excel2SBOL2 (2025-present)
James Nguyen - SynBioHub3 (2025-present)
Oscar Rodriguez - PUDU (2025-present)
Kenzo Schwab - SBOLCanvas (2025-present)
Ryan Greer - BuildCompiler (2024-present)
Peter Hindes - SynBioHub3 (2024-present)
Kerem Gurkan - SynBioSuite Frontend (2024-present)
Luke Dysart - PUDU (2025)
Taisiia Sherstiukova - Excel2SBOL2 (2024-2025)
Derick Sayavong - SBOLCanvas (2024-2025)
Bianca Gautum - SynBioHub2 (2023-2025)
Parker Ackerknecht - OpenTrons (2023-2025)
William Dravenstott - Excel2SBOL (2022-2025)
Zane Perry - SynBioHub3 Plugins (2022-2025)

Ima Mervin - SynBioHub2 (Fall 2024)
Maram Alaeai - SynBioHub Documentation (Summer 2024)
Rosalie Hughes - Experimental Setup GUI (Summer 2024)
Duncan Britt - SeqImprove (2023-2024)
Suhyun Bae - SBOLCanvas (2023-2024)
Dylan Smith - Data Repositories (2023-2024)
Samual Ball - Experimental Data Converter (2023-2024)
George Guo - SynBioHub3 (summer 2023)
Alex Elbel - SynBioHub3 (2022-2023)
Anjala Katuri - SynBioHub3 Testing (2022-2023)
Payton Thomas - iBioSim (2020-2023)
Benjamin Hatch - VisBOL and SynBioHub3 (2019-2023)
Zachary Sents - SynBioSuite (2022-2023)
Thomas Stoughton - iBioSim Server (2021-2022)
Julian Abam - ExcelSBOL Converter (2021-2022)
Eric Yu - SBOLExplorer and SynBioHub3 (2019-2022)
James Scholz - SynBioHub Testing (2019-2021)
CS Capstone Design Team (2019-2020)
Oliver Flatt - SynBioHub Testing
Samuel Bridge - SBOLDesigner
Nathan Wilkinson - VisBol
Igor Durovic - SBOL Library
Zach Zundel - SynBioHub
Tramy Nguyen - SBOL Library
Scott Glass - Flux Balance Analysis
Jason Stevens - Dynamic Modeling of Genetic Circuits
Hill Air Force clinic (2003-2008)
Curtis Madsen - Engineering Scholars Program
Nick Seegmiller - Engineering Scholars Program
Kip Killpack - A Low Power Digital Hearing Aid
Eric Mercer - SPAM Microprocessor Simulator
Brandon Bachman - SPAM Microprocessor Simulator
Robert Thacker - SPAM Microprocessor

Courses Taught

Engineering First Year Seminar (2024)

Engineering Genetic Circuits (2021,2022,2025)

Modeling and Analysis of Biological Networks (2003,2005,2007,2010,2013,2015,2017,2018)

Computer Design Laboratory (1999,2001,2012,2014,2019)

Fundamentals of Digital System Design (1999,2001,2014,2016,2019)

Asynchronous Circuit Design (1995,1997,2000,2001,2004,2006,2009,2011,2013,2015)

Formal Verification (1997,2012)

Embedded System Design (2004-2007, 2011)

Case Studies in CES (2008)

CE Junior Seminar (2006-2008,2018)

Hill Air Force Clinic (2003-2008)

CE Senior Thesis (2002)

Computer Aided Design of Digital Circuits (1996,1998,2000)

Hardware Fundamentals: Computer Organization and Design (1997-1998)

Microprocessor Laboratory (1996)

Courses Developed

1. Modeling and Analysis of Biological Networks - In 2009, I published the textbook, *Engineering Genetic Circuits*, used for this course. Published a three course specialization of this course on the Coursera Platform.
2. Asynchronous Circuit Design - In 2001, I published the textbook, *Asynchronous Circuit Design*, used for this course.
3. Computer Aided Design of Digital Circuits - This course provides an introduction to algorithms for the synthesis and optimization of digital designs.
4. Embedded System Design - I completely redesigned this course to focus on embedded system design issues rather than just interfacing with a PC.
5. Hardware Fundamentals - I completely redesigned a core course on hardware fundamentals and computer organization including adding new material to teach VHDL.
6. Formal Verification - This course presents state-of-the-art methods for the formal verification of hardware and software systems. A new version of this class was developed in 2012. Participating in the development of three 3-course specializations on this topic on the Coursera platform. Four of the nine courses have been delivered to date.

Publications and Patents

Books

1. C. J. Myers (translated by Li Peng), *Asynchronous Circuit Design* (in Chinese), Tsinghua University Press, September, 2013.
2. C. J. Myers, *Engineering Genetic Circuits*, Chapman & Hall/CRC Press, July, 2009.
3. C. J. Myers (translated by T. Yoneda), *Asynchronous Circuit Design* (in Japanese), Kyoritsu Shuppan, September, 2003.
4. C. J. Myers, *Asynchronous Circuit Design*, John Wiley and Sons, July, 2001.
5. J. Z. Lee, C. Campbell, and C. J. Myers, *Fate and Fortune in Rural China: Social Structure and Population Behavior in Liaoning*, Cambridge University Press, 1997.

Book Chapters and Books Edited

1. T. Novossiolova, B. Ellinport, C. Vindman, T. Binz, H. Jarman, C. Myers, M. Natsvlishvili, and M. Rojas, "Safeguarding the Responsible Use and Equitable Benefit-Sharing of Biotechnology in an Age of Scientific Modernization", in *Biotechnology and AI: Technological Convergence and Information Hazards*, pages 57-73, 2026.
2. T. Neupane, Z. Zhang, C. Madsen, H. Zheng, and C. Myers, "Approximation techniques for stochastic analysis of biological systems", in *Automated Reasoning for Systems Biology and Medicine*, pages 327-348, 2019.
3. C. Myers, K. Clancy, G. Misirli, E. Oberortner, M. Pocock, J. Quinn, N. Roehner, and H. Sauro, "The Synthetic Biology Open Language", in *Computational Methods in Synthetic Biology*, Methods in Molecular Biology, Volume 1244, pages 323-336, 2015.
4. C. Madsen, C. Myers, N. Roehner, C. Winstead, and Z. Zhang, "Efficient Analysis Methods in Synthetic Biology", in *Computational Methods in Synthetic Biology*, Methods in Molecular Biology, Volume 1244, pages 217-257, 2015.
5. A. Fisher, D. Kulkarni, and C. Myers, "A new assertion property language for analog/mixed-signal circuits", in *Languages, Design Methods, and Tools for Electronic System Design - Selected Contributions from FDL 2013*, Lecture Notes in Electrical Engineering, Volume 311, pages 45-65, 2015.
6. C. Myers, "Platforms for Genetic Design Automation", in *Methods in Microbiology 2013: Microbial Synthetic Biology*, November, 2013.
7. C. Myers (editor), *Stochastic Control*, Sciyo, August, 2010.
8. H. Kuwahara, C. Madsen, I. Mura, C. Myers, A. Tejeda, and C. Winstead, "Efficient stochastic simulation to analyze targeted properties of biological systems," in *Stochastic Control*, Sciyo, pages 505-532, August, 2010.
9. H. Kuwahara and C. J. Myers, "Abstraction methods for analysis of gene regulatory networks," in *Computational Methods in Gene Regulatory Networks*, IGI Global, pages 352-385, 2010.
10. E. Brunvand and C. Myers (editors), *2001 Conference on Advanced Research in VLSI*, IEEE Computer Society, March, 2001.
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46. C. Myers, R. Harrison, D. Walter, N. Seegmiller, and S. Little, "The case for analog circuit verification," in *Workshop on Formal Verification of Analog Circuits*, April, 2005.
47. T. Yoneda, A. Matsumoto, M. Kato, and C. J. Myers, "High level synthesis of timed asynchronous circuits," in *The Eleventh International Symposium on Asynchronous Circuits and Systems*, pages 210-218, March, 2005.
48. S. Little, D. Walter, N. Seegmiller, C. Myers, and T. Yoneda, "Verification of analog and mixed-signal circuits using timed hybrid Petri nets," in *Automated Technology for Verification and Analysis*, pages 426-440, November, 2004.
49. D. Pradubsuwun, T. Yoneda, and C. Myers, "Partial order reduction for detecting safety and timing failures of timed circuits," in *Automated Technology for Verification and Analysis*, pages 339-353, November, 2004.
50. T. Yoneda, H. Onda, and C. J. Myers, "Synthesis of speed independent circuits based on decomposition," in *The Tenth International Symposium on Asynchronous Circuits and Systems*, pages 135-145, April, 2004.
51. C. Nelson, C. Myers, and T. Yoneda, "Efficient verification of hazard-freedom in gate-level timed asynchronous circuits", in *2003 International Conference on Computer-Aided Design*, pages 424-431, November, 2003.
52. H. Zheng, C. Myers, D. Walter, S. Little, and T. Yoneda, "Verification of timed circuits with failure directed abstractions", in *IEEE International Conference on Computer Design*, pages 28-35, October, 2003.
53. C. Myers, E. Mercer, and H. Jacobson, "Verifying synchronization strategies", in *Formal Methods for Globally Asynchronous Locally Synchronous (GALS) Architecture*, September, 2003 (**Invited paper**).
54. T. Kitai, Y. Oguro, T. Yoneda, E. Mercer, and C. Myers, "Level oriented formal model for asynchronous circuit verification and its efficient analysis method," in *2002 Pacific Rim International Symposium on Dependable Computing*, pages 210-218, November, 2002.
55. T. Yoneda, T. Kitai, and C. Myers, "Automatic derivation of timing constraints by failure analysis," in *Computer Aided Verification, CAV '02*, pages 195-208, July, 2002.
56. C. Winstead, J. Dai, S. Yu, R. Harrison, C. Myers, and C. Schlegel, "Analog decoding of product codes" in *International Symposium on Information Theory*, June, 2002.
57. J. Dai, C. J. Winstead, C. J. Myers, R. R. Harrison, and C. Schlegel, "Cell library for automatic synthesis of analog error control decoders," in *2002 International Conference on Circuits and Systems*, volume 4, pages 481-484, May, 2002.
58. E. Mercer, C. J. Myers, T. Yoneda, and H. Zheng, "Modular synthesis of timed circuits using partial orders on LPNs," in *Theory and Practice of Timed Systems, TPTS '02*, April, 2002.

59. H. Jacobson, P. Kudva, P. Bose, P. Cook, S. Schuster, E. Mercer, and C. J. Myers, "Synchronous interlocked pipelines," in *The Eighth International Symposium on Asynchronous Circuits and Systems*, pages 3-12, April, 2002.

60. B. Zhou, T. Yoneda, and C. Myers "Framework of timed trace theoretic verification revisited," in *The Tenth Asian Test Symposium, ATS '01*, pages 437-442, November, 2001.

61. T. Yoneda, E. Mercer, and C. Myers, "Modular synthesis of timed circuits using partial order reduction" in *The Tenth Workshop on Synthesis and System Integration of MIxed Technologies (SASIMI 2001)*, October, 2001.

62. E. Mercer, C. Myers, and T. Yoneda, "Improved POSET timing analysis in timed Petri nets" in *The Tenth Workshop on Synthesis and System Integration of MIxed Technologies (SASIMI 2001)*, October, 2001.

63. C. Winstead, C. Myers, C. Schlegel, and R. Harrison, "Analog decoding of product codes" in *2001 IEEE Information Theory Workshop*, pages 131-133, September, 2001.

64. H. Zheng, E. Mercer, and C. J. Myers "Automatic abstraction for verification of timed circuits and systems," in *Computer Aided Verification, CAV '01*, pages 182-193, July, 2001.

65. C. Winstead, J. Dai, W. J. Kim, S. Little, Y.-B. Kim, C. Myers, and C. Schlegel, "Analog MAP Decoder for (8,4) Hamming code in subthreshold CMOS" in *2001 IEEE International Symposium on Information Theory*, page 330, June, 2001.

66. K. Killpack, E. Mercer, C. J. Myers, "A standard-cell self-timed multiplier for power and area critical synchronous systems" in *2001 Advanced Research in VLSI Conference*, pages 188-201, March, 2001.

67. C. Winstead, J. Dai, W. J. Kim, S. Little, Y.-B. Kim, C. Myers, and C. Schlegel, "Analog MAP Decoder for (8,4) Hamming code in subthreshold CMOS" in *2001 Advanced Research in VLSI Conference*, pages 132-147, March, 2001.

68. C. J. Myers and H. Jacobson, "Efficient exact two-level hazard-free logic minimization," in *The Seventh International Symposium on Asynchronous Circuits and Systems*, pages 64-73, March, 2001 **(Best Paper Finalist)**.

69. C. J. Myers, W. Belluomini, K. Killpack, E. Mercer, E. Peskin, and H. Zheng, "Timed circuits: a new paradigm for high-speed design", in *Asia and South Pacific Design Automation Conference 2001*, pages 335-340, February, 2001 **(Invited Paper)**.

70. H. Zheng and C. J. Myers, "Automatic abstraction for synthesis and verification of deterministic timed systems" in *2000 ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, December, 2000.

71. H. Jacobson, C. Myers, and G. Gopalakrishnan, "Achieving fast and exact hazard-free logic minimization of extended burst-mode gC finite state machines" in *2000 International Conference on Computer-Aided Design*, pages 303-310, November, 2000.

72. E. Mercer and C. J. Myers, "Stochastic cycle period analysis of timed circuits," in *2000 International Conference on Circuits and Systems*, volume II, pages 172-175, May, 2000.

73. S. T. Jung and C. J. Myers, "Direct synthesis of timed asynchronous circuits," in *1999 International Conference on Computer-Aided Design*, pages 332-337, November, 1999.

74. B. Bachman, H. Zheng, and C. Myers, "Architectural synthesis of timed asynchronous systems", in *IEEE International Conference on Computer Design*, pages 354-363, October, 1999.

75. E. Mercer and C. J. Myers, "Stochastic cycle period analysis of timed circuits," in *1999 International Workshop on Logic Synthesis*, June, 1999.

76. S. T. Jung and C. J. Myers, "Direct synthesis of timed asynchronous circuits," in *1999 International Workshop on Logic Synthesis*, June, 1999.

77. S. Rotem, K. Stevens, R. Ginosar, P. A. Beerel, C. J. Myers, K. Y. Yun, R. Kol, C. Dike, M. Roncken, and B. Agapiev, "RAPPID: An Asynchronous Instruction Length Decoder," in *The Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 60-70, April, 1999 (**Best Paper Award**).

78. W. Belluomini, C. J. Myers, and H. P., Hofstee, "Verification of Delayed-Reset Domino Circuits Using ATACS," in *The Fifth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 3-12, April, 1999.

79. W. Belluomini, C. J. Myers, and H. P., Hofstee, "Verification of Delayed-Reset Domino Circuits Using ATACS," in *1999 ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, March, 1999.

80. R. A. Thacker, W. Belluomini, and C. J. Myers, "Timed circuit synthesis using implicit methods," in *1999 12th VLSI Design Conference*, pages 181-188, January, 1999.

81. W. Belluomini and C. J. Myers "Verification of timed systems using POSETs," in *Computer Aided Verification, CAV '98*, pages 403-415, June, 1998.

82. W. Chou, P. Beerel, R. Ginosar, R. Kol, C. Myers, S. Rotem, K. Stevens, and K. Yun, "Average-case optimized technology mapping of one-hot domino circuits," in *The Fourth International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 80-91, April, 1998.

83. W. Belluomini and C. J. Myers, "Timed Event/Level Structures," in *1997 ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems*, December, 1997.

84. A. E. Sjogren and C. J. Myers, "Interfacing synchronous and asynchronous modules within a high-speed pipeline," in *17th Conf. on Advanced Research in VLSI*, pages 47-61, Sept, 1997.

85. R. A. Thacker and C. J. Myers, "Synthesis of timed circuits using BDDs," in *1997 International Workshop on Logic Synthesis*, May, 1997.

86. C. J. Myers and H. Zheng, "An asynchronous implementations of the MAXLIST algorithm," in *1997 International Conference on Acoustics, Speech, and Signal Processing*, volume 1, pages 647-650, April, 1997.

87. W. Belluomini and C. J. Myers, "Efficient timing analysis algorithms for timed state space exploration," in *The Third International Symposium on Advanced Research in Asynchronous Circuits and Systems*, pages 88-100, April, 1997.

88. C. J. Myers, P. A. Beerel, and T. H.-Y. Meng, "Technology mapping of timed circuits," in *2nd Working Conference on Asynchronous Design Methodologies*, pages 138-147, June, 1995.

89. C. J. Myers, T. G. Rokicki, and T. H.-Y. Meng, "Automatic synthesis of gate-level timed circuits with choice," in *1995 Chapel Hill Conference on Advanced Research in VLSI*, pages 42-58, March, 1995.

90. T. G. Rokicki and C. J. Myers "Automatic verification of timed circuits," in *Computer Aided Verification, CAV '94*, pages 468-480, June, 1994.

91. C. J. Myers and T. H.-Y. Meng, "Synthesis of timed asynchronous circuits," in *IEEE International Conference on Computer Design, ICCD-1992*, pages 279-284, October, 1992.

Invited Talks

1. COMBINE 2025, Madison, WI, October, 2025
2. IWBDA 2025, Worchester, MA, September 2025
3. CSHL Summer School on Synthetic Biology, New York, NY, July, 2024
4. NATO Workshop, Cartagena, Columbia, April 2024
5. DDECS 2024, Kielce, Poland, April 2024
6. IWBDA 2023, Boston, MA, September 2023
7. Banff Meeting, Banff, Canada, August 2023
8. SEED Conference Tutorial, Los Angeles, May 2023
9. Newcastle University, Newcastle, UK, May 2023
10. University of Rostock, Rostock, Germany, August 2022
11. Israeli SynBio Association Inaugural Conference, Herzliya, Israel, June 2022
12. SEED Conference Tutorial, Washington DC, April 2022
13. University of Minnesota, Virtual, December 2021
14. NSF Workshop on Systems and Control in Synthetic Biology, Washington DC, November 2021
15. SEED Conference, Virtual, June 2021
16. COMBINE Forum, Virtual, October 2020
17. 2020 International Workshop on BioDesign Automation, Virtual, July 2020
18. DARPA SD2 PI Meeting, Santa Barbara, CA, January 2020
19. Interagency Synthetic Biology Meeting, Washington D.C., October 2019
20. University of Cambridge, Cambridge, United Kingdom, October 2019
21. Shonan, Tokyo, Japan, September 2019
22. COMBINE Forum, Heidelberg, Germany, July 2019
23. Imperial College London, London, United Kingdom, July 2019
24. Oxford Synthetic Biology CDT Symposium, Oxford, United Kingdom, July 2019
25. BioRoboost, Madrid, Spain, June 2019
26. Oxford Global Synthetic Biology Congress, London, United Kingdon, November 2018
27. SB4D Workshop, Arlington, VA, September 2018
28. CMSB 2018, Brno, Czech Republic, September 2018
29. University College London, London, United Kingdom, September 2018
30. NSF Living Computing Project Site Visit, Boston, MA, August 2018
31. SBOL Developers Workshop, Berkeley, CA, July 2018
32. DARPA SD2 PI Meeting, Seattle, WA, July 2018
33. ASYNC 2018, Vienna, Austria, May 2018
34. Dagstuhl Seminar, Germany, March 2018
35. University of Nebraska, Lincoln, NE, October 2017
36. Technical University of Denmark, Copenhagen, Denmark, October 2017
37. SBOL Developers Workshop, Pittsburgh, PA, August 2017
38. SEED Conference, Vancouver, Canada, June 2017
39. Massachusetts Instistute of Technology, Cambridge, MA, May 2017
40. Boston University, Boston, MA, May 2017
41. BBN/Raytheon, Cambridge, MA, April 2017
42. Microsoft Research, Cambridge, UK, March 2017

43. Newcastle University, Newcastle, UK, March 2017
44. University of Oxford, Oxford, UK, March 2017
45. University of Bristol, Bristol, UK, February 2017
46. Imperial College London, London, UK, February 2017
47. SynBioUK 2016, Edinburgh, UK, November 2016
48. University of Oxford, Oxford, UK, November 2016
49. Newcastle University, Newcastle, UK, October 2016
50. COMBINE Workshop, Newcastle, UK, September 2016
51. SBOL Workshop, Newcastle, UK, August 2016
52. HARMONY Workshop, Auckland, New Zealand, June 2016
53. IWBDA, Seattle, WA, August 2015
54. VEMDP Workshop, San Francisco, CA, July 2015
55. Verimag, Grenoble, France, June 2015
56. Inria, Grenoble, France, June 2015
57. HARMONY Workshop, Wittenberg, Germany, April 2015
58. SY-BIO Workshop, Dallas, Texas, March 2015
59. RWTH Aachen, Aachen, Germany, March 2015
60. Whole Cell Summer School, Rostock, Germany, March 2015
61. ICSB Workshop on Standards, Melbourne, Australia, September 2014
62. ICSB Tutorial, Melbourne, Australia, September 2014
63. COMBINE Workshop, Los Angeles, CA, August 2014
64. SEED Conference, Los Angeles, CA, July 2014
65. Inria, Grenoble, France, July 2014
66. HARMONY Workshop, Manchester, UK, April 2014
67. University of California, Davis, CA, January 2014
68. COMBINE Workshop, Paris, France, September 2013
69. International Workshop on Bio-Design Automation, London, UK, July 2013
70. Synthetic Biology 6.0, London, UK, July 2013
71. Design Automation Summer School, Austin, TX, June 2013
72. University of Connecticut Health Science Center, Farmington, CT, May 2013
73. Newcastle University, Newcastle, UK, April 2013
74. University of South Florida, Tampa, CA, April 2013
75. National Tsing Hua University, Hsinchu, Taiwan, March 2013
76. National Taiwan Univ., Genome and Systems Biology Center, Taipei, Taiwan, March 2013
77. Academia Sinica, Nankang, Taiwan, March 2013
78. National Taiwan University, EECS, Taipei, Taiwan, March 2013
79. Workshop on Design Automation for AMS, San Jose, CA, November 2012
80. ICCAD, San Jose, CA, November 2012
81. COMBINE Workshop, Toronto, Canada, August 2012
82. CAV Tutorial, Berkeley, CA, July 2012
83. RWTH Aachen, Aachen, Germany, May 2012
84. Cornell University, Ithaca, NY, April 2012
85. Intel Corporation, Portland, OR, December 2011

86. COMBINE Workshop, Heidelberg, Germany, September 2011
87. International Conference on Systems Biology Tutorial, Heidelberg, Germany, September 2011
88. Design Automation Summer School, San Diego, CA, June 2011
89. Workshop on Diversity in Design Automation and Test, Pittsburgh, PA, May 2011
90. Dagstuhl Seminar, Germany, April 2011
91. SRC Verification Review, Santa Barbara, CA, April 2011
92. Microsoft Research Cambridge, United Kingdom, October 2010
93. Intel Corporation, Portland, OR, July 2010
94. Dagstuhl Seminar, Germany, July 2010
95. Carnegie Mellon University, Pittsburgh, PA, December 2009
96. Brigham Young University, Provo, UT, November 2009
97. ICCAD Tutorial, San Jose, CA, November 2009
98. CANDE Workshop, Monterey, CA, October 2009
99. Intel Corporation, Portland, OR, October 2009
100. First RoSBNet Synthetic Biology Workshop, Oxford, United Kingdom, September 2009
101. Technical University of Denmark, August 2009
102. Utah State University, Logan, UT, July 2009
103. International Workshop on Bio-Design Automation, San Francisco, CA, July 2009
104. NSF Workshop: EDA-Past, Present, and Future, Washington D.C., July 2009
105. SRC Verification Review, Raleigh, NC, April 2009
106. Caltech, March 2009
107. University of California, Berkeley, October 2008
108. Technical University of Kaiserslautern, Germany, September 2008
109. Dagstuhl Seminar, Germany, September 2008
110. International Conference on Systems Biology Tutorial, Gothenburg, Swedwn, August 2008
111. International Workshop on Logic Synthesis, Lake Tahoe, CA, June 2008
112. IMA Workshop, Minneapolis, MN, April 2008
113. SRC Verification Review, Berkeley, CA, March 2008
114. Banbury Workshop, Cold Spring Harbor, NY, May 2007
115. SRC Verification Review, Salt Lake City, UT, April 2007
116. University of California, Berkeley, CA, March 2007
117. Cadence Berkeley Labs, Berkeley, CA, March 2007
118. EPFL, Laussane, Switzerland, June 2006
119. NSF/ECS Grantees Workship, Tuskegee, AL, June 2006
120. University of Southern California, May 2006
121. SRC Verification Review, Pittsburgh, PA, April 2006
122. David Evans Conference on CE, Heber City, UT, May 2005
123. Caltech, May 2005
124. SRC Verification Review, Boulder, CO, March 2005
125. Southern Taiwan University of Technology, Tainan, Taiwan, November 2004
126. Brigham Young University, November 2004
127. Kitano Symbiotic Systems Group, Tokyo, June 2004
128. SRC Verification Review, Princeton, NJ, March 2004

129. BioMath Seminar, U. of Utah, December 2003
130. Bioengineering Seminar, U. of Utah, September 2003
131. FMGALS 2003, September 2003
132. Human Genome Center, U. of Tokyo, May 2003
133. Research Center for Advanced Science and Technology, U. of Tokyo, May 2003
134. SRC Verification Review, Austin, TX, April 2003
135. UC Berkeley, February 2003
136. Stanford University, February 2003
137. David Evans Conference on CE, Heber City, UT, June 2002
138. SRC Verification Review, Salt Lake City, UT, March 2002
139. SRC Verification Review, Pittsburgh, PA, March 2001
140. ASP-DAC 2001, February 2001
141. Lucent Technologies, November 2000
142. Sonic Innovations, September 2000
143. SUN Microsystems, June 2000
144. SRC Verification Review, Austin, TX, March 2000
145. Caltech, March 2000
146. Asynchronous design tutorial for Samsung, July 1999
147. SRC CAD Review, Irvine, CA, March 1999
148. ASYNC98, CAD demo, San Diego, CA, April 1998
149. SRC CAD Review, Austin, TX, March 1998
150. IBM Austin Research Laboratory, June 1997
151. Stanford University, May 1997
152. Technical University of Denmark, April 1997
153. University of Manchester, April 1997
154. ASYNC97, CAD demo, Eindhoven, Netherlands, April 1997
155. Intel Portland, August 1996
156. Caltech, May 1996
157. 3-day short course on asynchronous design, Intel Portland, April 1996
158. ASYNC96, CAD demo, Aizu, Japan, March 1996
159. Beijing Institute of Machinery, March 1996
160. Intel Portland, September 1995
161. Intel Israel, August 1995
162. Phillips Nat Lab in Eindhoven, Netherlands, June 1995
163. IMEC in Leuven, Belgium, June 1995
164. University of Manchester, June 1995
165. SUN Microsystems, April 1995